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Voltage Measurements techniques comparison in VCO low consumption circuits

Luiz Fernando Viera Costa
Pablo Gonçalves Nascimento

PUC RIO

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Students: Luiz Fernando Viera Costa

Pablo Gonçalves Nascimento

Advisor: Adriano F. Branco

Work presented as partial requirement to the conclusion of the Engenharia Elétrica major in the Pontifícia Universidade Católica do Rio de Janeiro, Rio de Janeiro, Brasil.

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Abstract

This work aims to experiment with logical gates-based low-power voltage measurement circuits as a feasible alternative for Energy Harvesting applications. The motivation for doing so is to evaluate this energy measurement method in low-energy scenarios, in order to observe its accuracy and power consumption. In this kind of application, the stored energy level is relevant because it is not abundant, so energy efficiency is essential in every step. Our conclusion is that the use of discrete circuits for the VCO model presented by the Failure Sentinels work is unlikely to be fully implemented using the currently available discrete components in the market, especially for lower voltage values.

Keywords: Energy Harvesting, energy measurement, VCO, ADC, Comparator

Comparação de Técnicas para Medição de Tensão em circuitos VCO de baixo consumo

Resumo

O objetivo do projeto é realizar experimentos com o circuito medidor de tensão VCO baseado em portas lógicas visando baixo consumo como uma alternativa viável para aplicações de ENergy Harvesting. A motivação dessa comparação é avaliar esse método de medição de energia para aplicações de baixa potênciam de modo a observar sua precisão e consumo. Nesse tipo de aplicação o nível de energia armazenada é importante, vito que ela não é abundante, então a eficiência energética nos procedimentos é fundamental. Nós concluímos que o uso de componentes discretos para utilização no modelo VCO apresentado no Failure Sentinels é altamente improvável de ser plenamente implementado com os componentes atualmente disponíveis.

Palavras-chave: Colheita de Energia, Medição de energia, VCO, ADC, Comparador

Summary

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1 Introduction

The recent and rising growth of IoT devices used around the world [1] illustrated in Figure 1 leads to several problems, particularly regarding energy availability. Focusing on embedded systems, the usual first power supply solution is batteries. However, that requires many of those to supply all devices, apart from replacing them when the batteries become discharged. This replacement problem also raises environmental questions, such as battery manufacturing and discarding processes. Besides, if these IoT devices are on remote sites, reaching them to replace their battery would also be a problem, increasing the replacement cost, which tends to get more expensive [2].

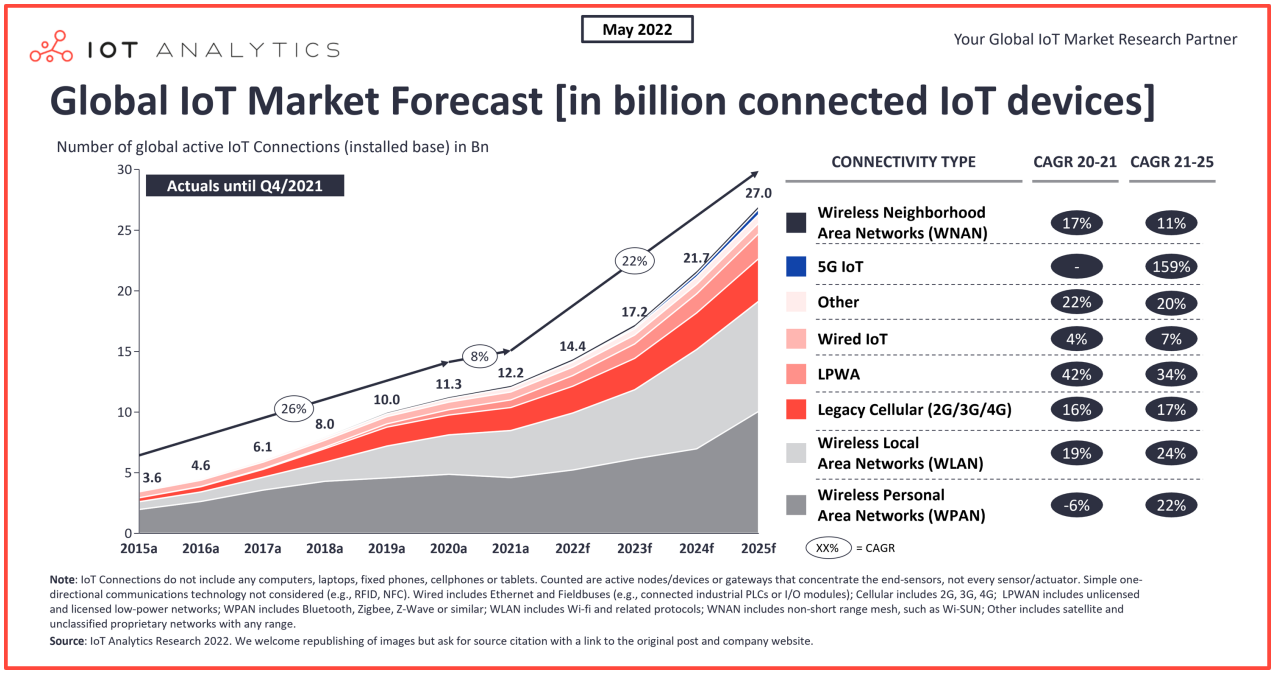


Figure 1: Global IoT market forecast
Mohammad Hasam [1]

To avoid all previously listed problems, a possible strategy is *Energy Harvesting* (EH). The overall idea of this concept is to use the energy in the environment to generate electrical energy through transducers, which can be solar, radio frequency, thermoelectric [3], piezoelectric [4], or magnetic [5], as shown in Figure 2. Although EH solves battery environmental and logistical issues, it also has its challenges, where energy intermittency plays a significant role.

The intermittency happens due to the intermittent nature of the sources. For instance, this is an inherent problem regarding solar energy harvesting since no solar light is available at night. Devices with that power source would be in trouble working after twilight. Even when energy sources are not intermittent, they can generate insufficient power, which needs to be stored until there is enough energy [6]. This issue can occur in a radio frequency energy harvesting application, for example, in a site where the radiowaves attenuation is significant enough to make them insufficient to provide the required power. In both cases, energy storage is a possible solution, but how it is done depends on the case since energy harvesting is explicitly developed for its applications.

These intermittent devices' hardware usually includes a microcontroller (MCU) or even a CPU, sensors, volatile and non-volatile memories, and radios for communication. Their software also runs intermittently, executing when there is energy until it is over and then resuming execution when energy becomes available again [6].

To keep the program running intermittently, it is necessary to keep tracking its execution. To do so, the system has to save the program context before running out of power to restart it from that point when the energy is back. A naive strategy to solve this problem is saving context for every MCU instruction or program block, but this leads to spending energy to save contexts that will be overwritten. Therefore, a more thoughtful strategy is to save the program context after the available energy is under a threshold but to do so, it is required to measure the stored energy. Consequently, ADCs or voltage comparators

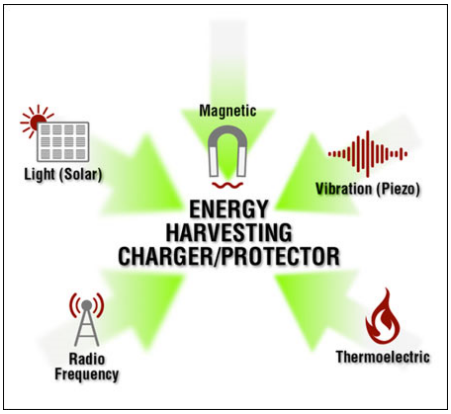


Figure 2: Energy Harvesting sources
Analog Devices [7]

may be used to address this problem since it is easier to measure the energy.

Energy monitoring is an essential topic in Energy Harvesting, being a base of charge control interface that monitors available energy and defines how to store it. This concept is based on the necessity of determining how much energy is available to use and how to store it when it is not possible to harvest any more energy. Since energy is not constantly available or abundant, it must be efficiently used to ensure enough power to execute the device's main tasks.

In this context, Failure Sentinels [8] was also developed to leverage the propagation delay response of logical gates to voltage supply fluctuation predictability to measure available energy. Our work aims to validate Failure Sentinels results and feasibility by replicating it in the original layout and using discrete devices.

2 Literature Review

The Energy Harvesting state-of-art demonstrates there are two primary contexts regarding this topic. These contexts are the charge control interface and program execution control. The execution control focuses are strategies for program execution and progress, which is the software perspective. The charge control interface, on the other hand, is concerned with controlling the charging system, from energy-storing methods to how monitoring the amount of energy available.

Regarding the energy perspective, the basic strategy is not storing energy. In that case, the device runs just when harvesting energy is available, potentially generating several powerless gaps. Besides, if the device does not totally use the harvested energy, it is wasted since it is not stored.

Another strategy is to use the harvested energy to recharge a battery, as used in the Singpost Platform [9], where the energy from the solar panels is stored in the battery so the modules can be supplied in the desired voltages, as shown in Figure 3.

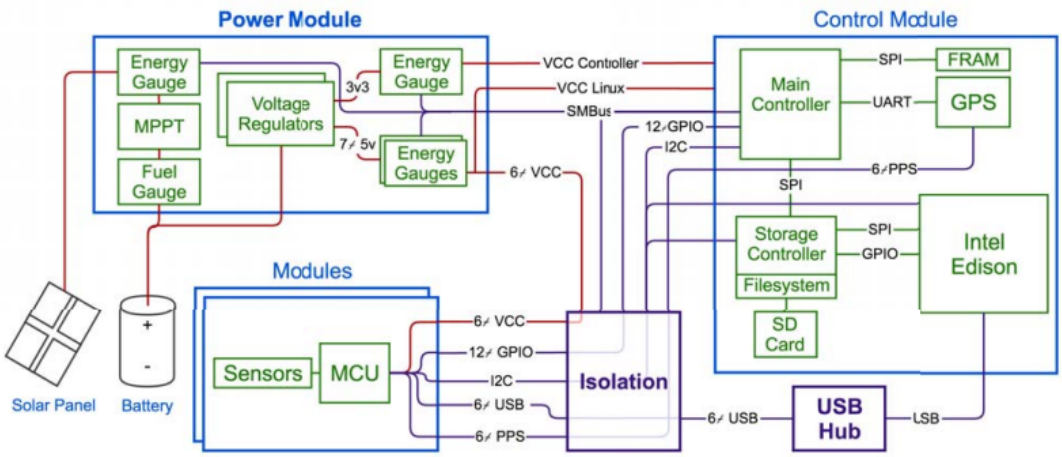


Figure 3: Signpost architecture
Joshua Adkins et al. [9]

However, using batteries would not only reinstate all problems listed in Section 1 but also have some limitations according to the applications, such as physical size, fire or explosion risk [8], or even not working correctly in high humidity [10] or extreme temperature [11] environments.

It is possible to use capacitors to avoid using batteries but still store energy. For instance, Ikeda et al. [12] proposed a battery-free soil-monitoring sensor powered by a thermoelectric generator (TEG) for agriculture applications with two main capacitors: C_{OUT}, responsible for supplying the load required current, and C_{STORE}, which actually stores energy for powering the system when there is no harvested energy.

Another interesting example is a work in which the authors proposed an ”intermittently-powered energy harvesting step counter for integrated wearable applications, which aims to remove the energy storage element” (Rodriguez et al., 2017). Indeed, their implementation did not use an explicit energy storage element, but the capacitor from the voltage rectifier indirectly plays that role so that it may seem more like a capacitor-based system [13].

Finally, it is possible to use supercapacitors, similar to Qi et al. [14], who proposed a self-sustainable water quality sensor powered by the magnesium oxidizing microorganisms (MOMs) present in the same water using three supercapacitors in parallel to supply their sensor module with 1v stable from the 0.33v and 400μ harvested power.

Once the energy is stored, it may be used to supply the microcontroller. However, the MCU needs to be able to deal with intermittency since energy harvesting is not continuous nor entirely predictable. Therefore, during program execution, it is essential to know how much power the device has available to trigger an action to store the memory states regarding the program execution (program context). We call *taking a snapshot* this saves context action. When that device has enough power to resume program execution, it uses this snapshot to recover its state and continue its tasks where it left off [6]. Since the energy available is not abundant, the energy measuring process needs to consume the lowest power possible, which is another reason to understand and compare the energy monitoring methods.

After discussing the energy storing strategies, it is necessary to understand the four main methods of monitoring that energy, accordingly to Energy Harvesting state-of-art. These methods are: using the MCU internal ADC, using an external ADC, using the MCU internal comparator, or using an external comparator.

Ransford et al. designed Mementos [15] to convert regular programs into interruptible ones. For that purpose, they implemented energy-measurement routines at control points in the code alongside a library to support the required functions. In hardware terms, the system development focused on using the MSP430F2132 microcontroller, which has an on-chip ADC, allowing the authors to use it.

Similarly, Jayakumar et al. designed "an energy-aware memory mapping technique that maps different program sections to the hybrid FRAM-SRAM microcontroller such that energy consumption is minimized without sacrificing reliability" [16]. The eM-Map, as it was called, also used an MSP430-series MCU, more specifically an MSP430FR5739, because it has a hybrid FRAM-SRAM memory but also provides the onboard ADC to measure the supply voltage consuming less than 5μJ.

In Ruppel et al. Culpeo-R-ISR implementation, the ADC sampling power consumption went from 4.2% to 0.003% by changing from the MSP430 on-chip ADC to an external 8-bit converter [17].

Culpeo-μArch is the microarchitecture that measures the capacitor responsible for storing energy voltage with an 8-bit ADC alongside a digital comparator to capture the minimum or maximum voltage, as illustrated by Figure 4. In that diagram, "red arrows indicate inputs, solid arrows are analog signals, dashed arrows are boolean and wide arrows are 8-bit buses" (Ruppel et al.,2022).

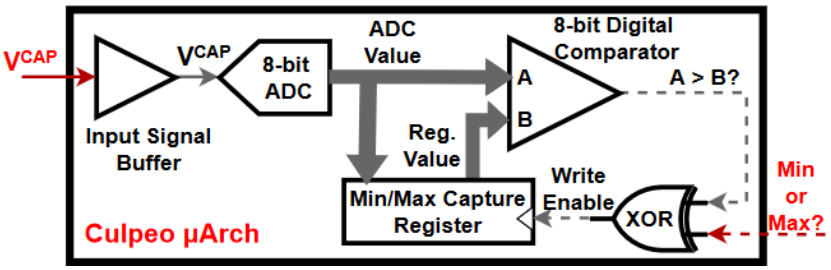


Figure 4: Culpeo-μArch
Ruppel et al. [17]

The internal ADC strategy uses the chip's onboard ADC to measure available energy. Since it's simple, it is a usual solution. On the other hand, the external ADC strategy adds an ADC to the circuit since its measurement demands less power, but it increases the circuit complexity.

Alternatively, Balsamo et al. [18] evaluated the consumption for executing the Fast Fourier Transform algorithm of three arrays with 128 8-bit samples each. The experiment used the MSP430FR5739 microcontroller onboard ADC and comparator and measured 310 μW and 130 μW power consumption, respectively, at mid-range from the maximum and minimum voltage of the algorithm.

Furthermore, Balsamo et al. [18] proposed Hibernus, an approach that saves a snapshot as soon supply voltage is below the hibernation threshold voltage. Once hibernating, the device is only awakened after surpassing the restoration threshold voltage. Figure 5 shows the described Hibernus operation accordingly to an intermittent supply voltage level. However, both threshold levels are arbitrarily set, which demands precise calibration to avoid wasting computation time.

In the following work, Balsamo et al. upgraded Hibernus, creating Hibernus++ [19], illustrated in Figure 6, which self-calibrates its hibernation and restores threshold value. Another improvement was to replace the MSP430FR onboard comparator with an external comparator, shown in Figure 7, reducing the comparative power consumption by over an order of magnitude.

Finally, Williams et al. [8] designed Failure Sentinels to leverage digital logic gates' predictable propagation delay response to supply voltage fluctuations to measure available energy. In other words, it is a VCO (Voltage Circuit Oscillator) formed by a RO (Ring Oscillator), which is a NOT digital gates chain. The main idea is to measure the available energy through the oscillation frequency in RO using a counter, which differs from the previously described methods.

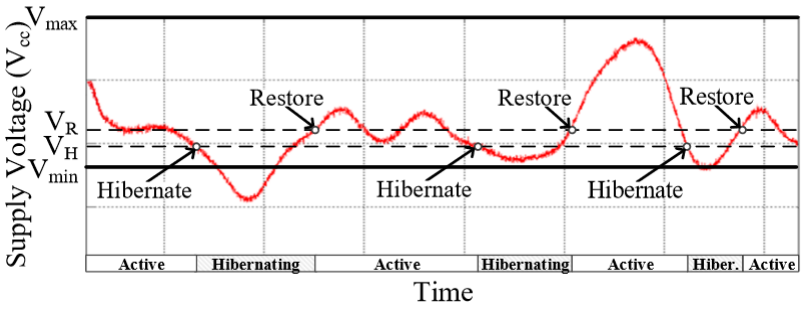


Figure 5: Hibernus
Balsamo et al. 2015 [18]

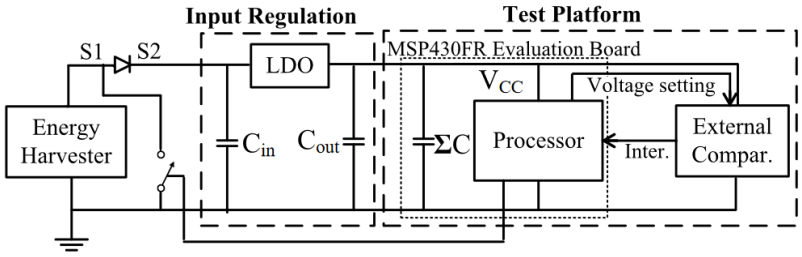


Figure 6: Hibernus++
Balsamo et al. 2016 [19]

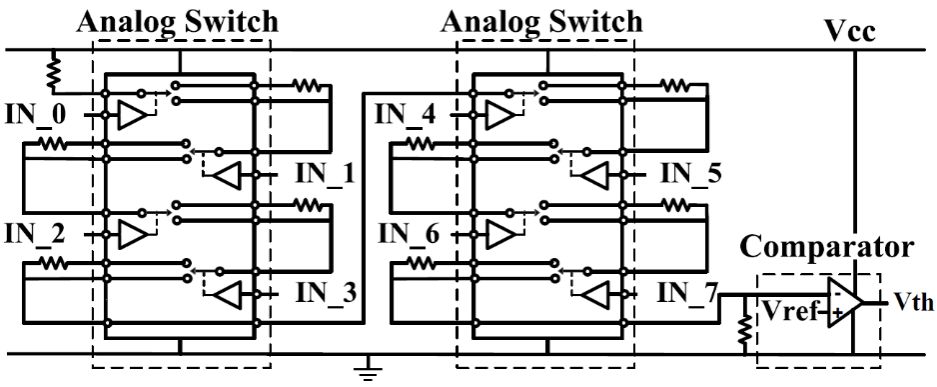


Figure 7: Hibernus++ external comparator
Balsamo et al. 2016 [19]

3 Methodology

Since Failure Sentinels is strictly different from the most known energy measuring strategies presented in Chapter 2, we decided to evaluate its performance by testing a 7-staged Ring Oscillator for the 0.2 to 3.6 V voltage range to verify the actual topology power consumption. However, since this topology was designed to be lithographically printed, it is not feasible to reproduce it with our resources. To overcome this limitation, we used LTspice [20] as a reliable alternative to simulate and measure the characteristics of the original circuit.

Discrete components give us insights into the circuit's behavior and identified differences from the lithographic implementation, since we have to match the circuit requirements with the available devices in the market. This approach allows us to compare the results obtained with Failure sentinels simulation results, even without lithographic printing capabilities.

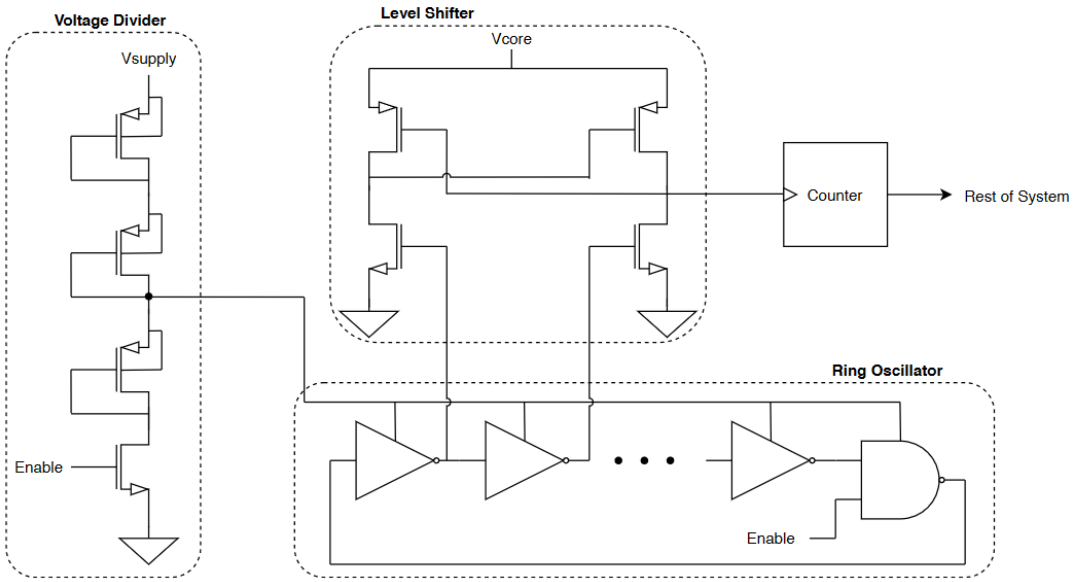


Figure 8: Failure Sentinels block diagram
Williams et al. [8]

Figure 8 presents the Failure Sentinels block diagram, where there are three main blocks. The first one is the Voltage Divider block, which provides a proportional lower voltage to the Ring Oscillator block from the supply voltage. In the Ring Oscillator block, there are 5 NOT logical gates in the block's core besides a NAND gate, which counts as two stages in the ring, since there are two propagation delays in that gate. It oscillates at a lower voltage from the divider because it generates lower switching noise jitter and consumes less power.

a Original Layout

Before highlighting the circuits' specific details, it is necessary to clarify the methodology responsible for generating the results presented in the paper. Since the author aimed to evaluate how the length would impact the Ring Oscillator sensibility, he implemented several programs to execute all steps, from elaborating the circuit netlist to plotting the results. All programs mentioned here are available on the author's repository [21].

Figure 9 presents the Failure Sentinels program block diagram. Firstly, the `Ring Oscillator` program generates the circuit netlist from components parameters, such as width, internal capacitances, and resistances. This algorithm receives some parameters by `Generate Netlist`, which suggestively generates the circuit netlist according to the ring oscillator size, supply and core voltages, and Monte Carlo method [22] parameters given to `Ring Oscillator`.

After generating the netlist, `Mt Runner` executes LTSpice based on it, obtaining the results. Then, frequency reads the file created by `Mt Runner` and calculates operation frequency, power, and voltage output amplitude values, besides mean value, error, and standard deviation data for each measurement. The following step

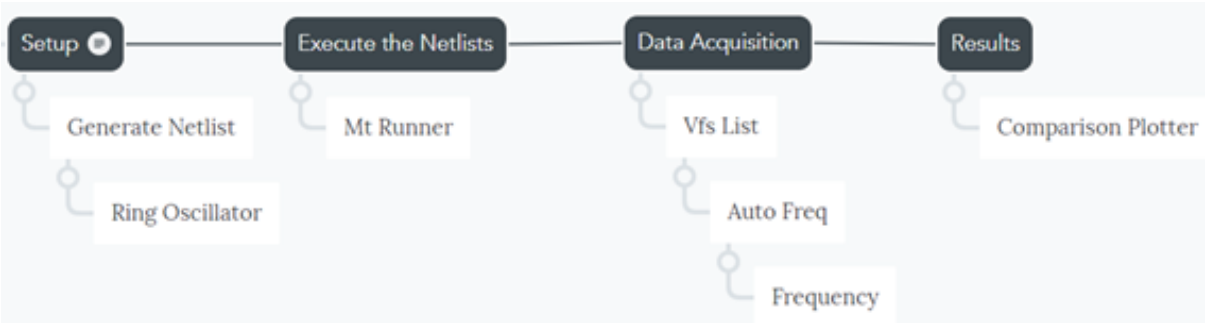


Figure 9: Failure Sentinels programs block diagram

is to use `Auto Freq` to provide the path to the file created on `Mt Runner` execution, which also demands the creation of a .csv file containing all data outputs for each parameter given by `Generate Netlist`.

Once the user saves the `Mt Runner` data outputs file as a .csv file, `Vfs List` loads this file to create a voltage-frequency relation according to it, which also must be saved by the user after inserting a column containing the component's width. Finally, `Comparison Plotter` loads this file and plots the frequency-voltage relations and sensibility graphics.

It is noticeable that this is not the standard approach to electronic engineering problems. Therefore, it was first necessary to replicate the original circuit, observing the electronic aspects that will further be evaluated. With the Voltage Divider, Ring Oscillator, and Level Shifter blocks in mind from the diagram presented in Figure 8, we analyzed the netlist created, and we concluded it is possible to subdivide the Ring Oscillator in Enable Circuit and Ring Oscillator Core. These subcircuits enable the Ring Oscillator operation and the proper Ring Oscillator.

Besides the blocks, there are three voltage sources named V_{core}, V_{supply} and V_{enable} representing the MCU's minimum operation voltage, system's supply voltage, and circuit enable signal from microcontroller, respectively. As from the netlist and these modules identification, it was possible to design the circuit's schematics for a 7-stage RO presented in Figure 10.

After drawing the complete schematics, it is feasible to investigate each circuit block to understand them fully. All blocks use different enhancement-type MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) arrangements. This kind of device is also categorized accordingly to its manufacturing into NMOS and PMOS. The p-type substrate n-channel MOSFET is named NMOS, and the n-type substrate p-channel MOSFET is called PMOS [23].

MOSFET ideal operation occurs when a potential difference between gate and source induces a channel in the substrate, where a current I_d flows. Figure 11 illustrates that operation for an NMOS transistor [23].

Finally, from an NMOS-PMOS junction, it is formed a CMOS (Complementary Metal-Oxide Semiconductor), as shown in Figure 12. This topology is relevant because it operates as a digital logic inverter, where the gate is the input and the drain the output, which explains why it was used in Failure Sentinels [23].

The first block to be discussed is the Voltage Divider, where the supply voltage V_{supply} is divided by three, and then it is provided to the Ring Oscillator block. This voltage downsizing was designed to reduce the RO power consumption and the RO's output signal ripple. In hardware terms, the Voltage Divider block consists of three PMOS and one NMOS, connected as illustrated in Figure 13.

This module is activated when $Enable$ is at 1.8 V, receiving this voltage from MCU, represented by V_{Enable} source. Regarding the output, V_{div} is the voltage sent to RO, which is given by Equation 1 since the 3 PMOSes have identical transconductance and output resistance values due to having the same parameters [24].

$$V_{div} = \frac{V_{Supply}}{3} \tag{1}$$

The Enable sub-circuit activates the RO core by inputting the enable reference voltage to the NAND logic gate, which is prevenient from V_{Enable} source. The other NAND gate input is $V_{0_{in}}$, whose origin is the RO feedback signal. The Voltage Divider block also supplies voltage to this sub-circuit. That NAND logic gate is also implemented with CMOS, as shown in Figure 14.

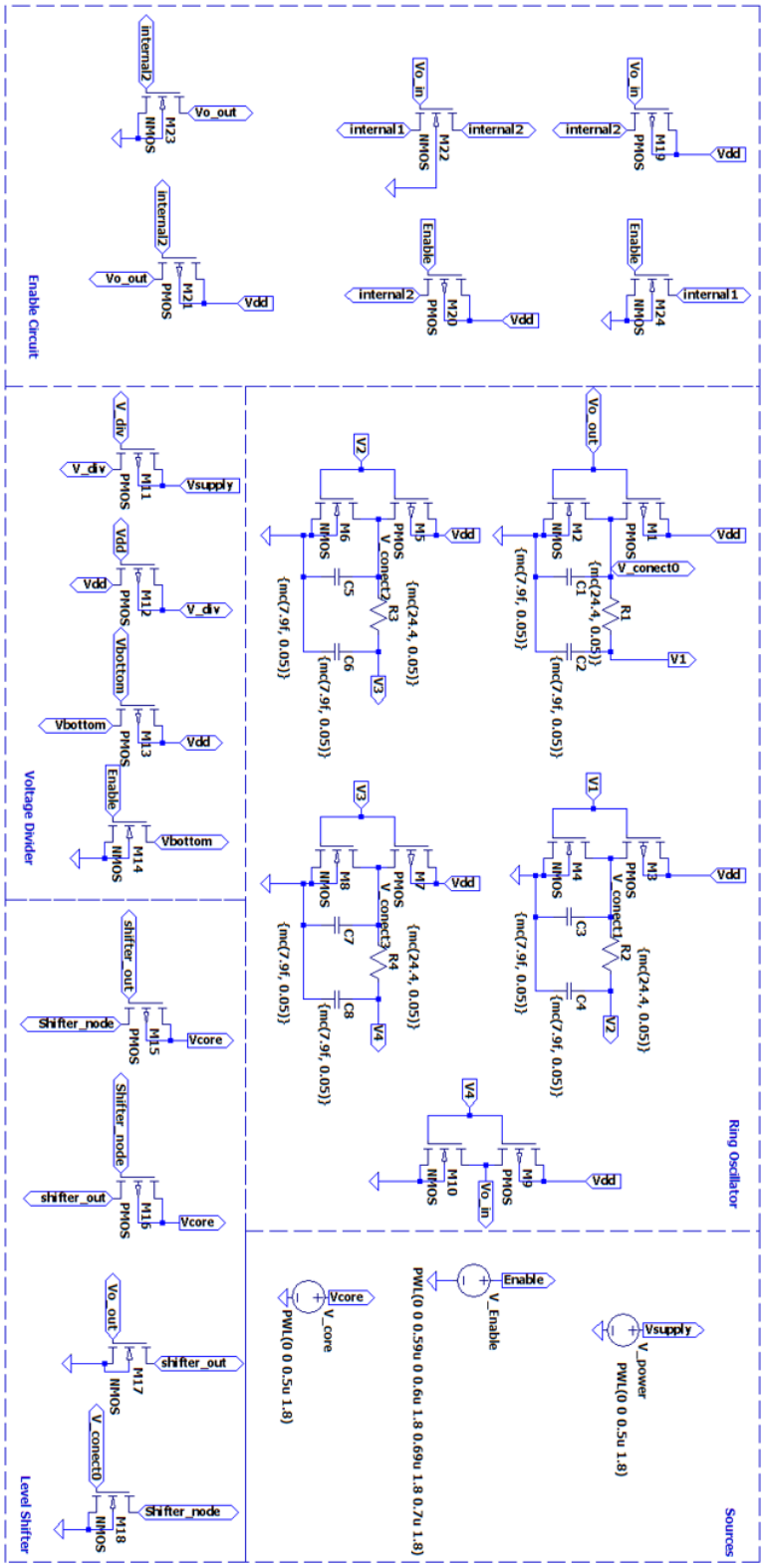


Figure 10: 7-staged RO Complete Schematics

Failure Sentinels implemented the NAND gate in two stages. First, the authors implement the NOT logical gate with the CMOS created by combining the PMOS M19 and NMOS M22 presented in Figure 14. Then, the CMOS composed by PMOS M21 and NMOS M23, also shown in the same image, implements the AND stage, which outputs $V_{0_{out}}$ and connects to the RO core. Since there are two steps in this NAND gate

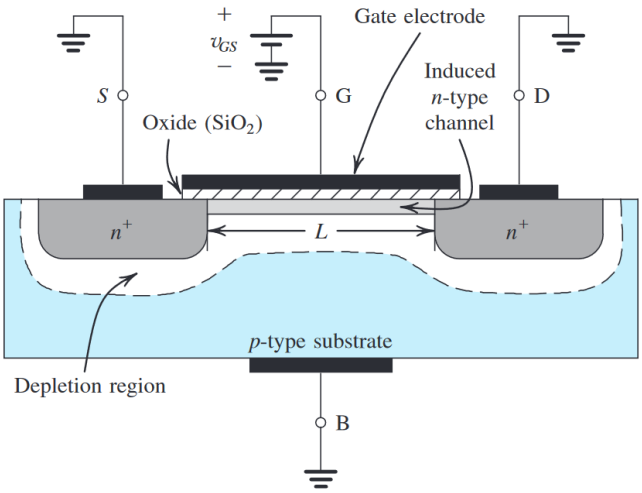


Figure 11: Enhancement-type NMOS transistor
Sedra et al. [23]

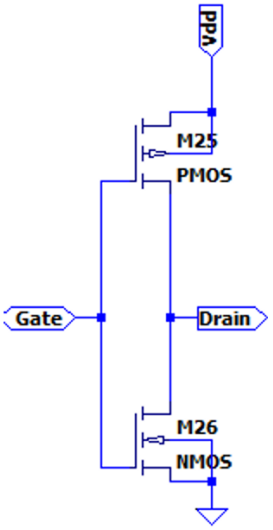


Figure 12: CMOS topology

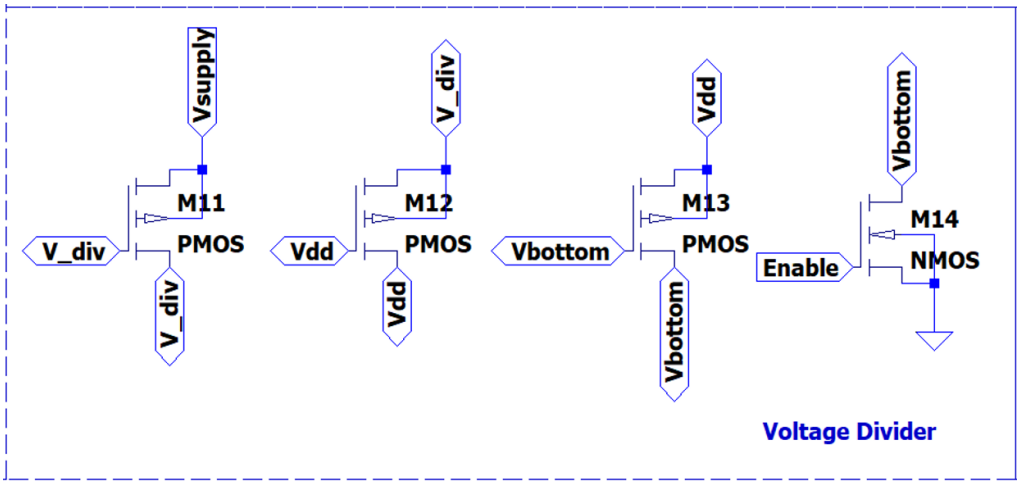


Figure 13: Failure Sentinels Voltage Divider block

implementation, it counts as two of the seven RO stages once the enabled circuit is a Ring Oscillator block subcircuit.

The RO core subcircuit shown in Figure 15 converts most of the input voltage into frequency. As previously said, the Voltage Divider block supplies this subcircuit, and the Enable subcircuit activates the RO by closing the ring in $V_{0_{in}}$, also presented in Figure 15. Failure Sentinels also designed resistive and capacitive components in interconnections between CMOSes to simulate parasite resistance and local interconnections estimates to these components' technology.

The Level Shifter module shown in Figure 16 generates a 1.8 V pulse, the most minor MCU reference voltage used by Failure Sentinels, and consists of a CMOS pair that receives the $V_{0_{out}}$ and $V_{connect0}$ voltages from the RO block. These voltage values allow measuring the propagation delay in a CMOS gate or, in other words, a RO stage. However, hence the oscillation voltage is only the V_{supply} third part, as given by Equation 1, and the supply voltage varies from 0.2v to 3.6v. It is mandatory to amplify the oscillation voltage to minimize the frequencies jitter as possible. Unlike the other modules, the Level Shifter block supply is V_{core}, provided from MCU as a 1.8v voltage. Finally, its output is the $shifter_{out}$ 1.8v signal whose frequency is defined as the propagation delay observed from the RO block.

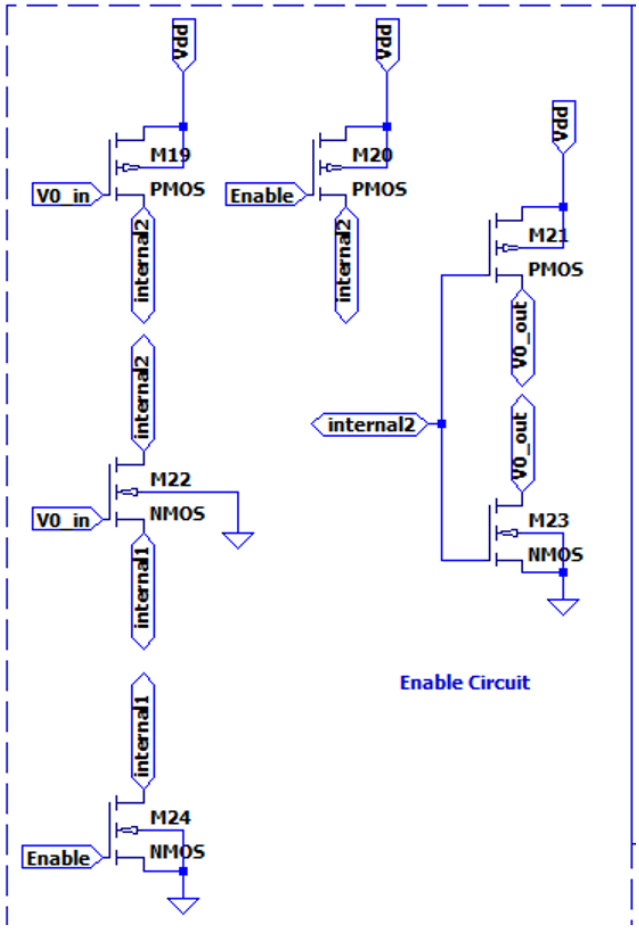


Figure 14: Failure Sentinels Enable Circuit

b Discrete Layout

Once we fully understood the original layout, we could finally discretize the design to make its manufacturing feasible for most researchers. Initially, we looked for CMOS chips, preferentially allowing access to MOSFETs substrate, known as enhancement-type. That is a required feature because the original design also used this property, especially with the NAND gate, where there is a connection between an NMOS substrate and a different source terminal.

The first chip found with that characteristics was CD4007UB [25] that is a Texas Instruments CMOS dual complementary pair plus inverter with the functional diagram shown in Figure 17. However, its datasheet pointed out some performance issues that must be mentioned. First, the device's minimum supply voltage is 3v, but the required potential difference to operating as a RO is 3.3 V since input and output protection circuit losses exist.

It is also pertinent that the circuit uses diodes and resistors, which makes it unfeasible to implement a voltage divider as the maximum range value of 3.6v would be so close to the 3.3v used, reducing the circuit resolution. However, features like input capacitance, propagation delay, transition time, and input current are relatively low, besides the 500mW chip and 100mW CMOS pair consumption [25]. Figure 18 illustrates the CD4007UB internal schematics.

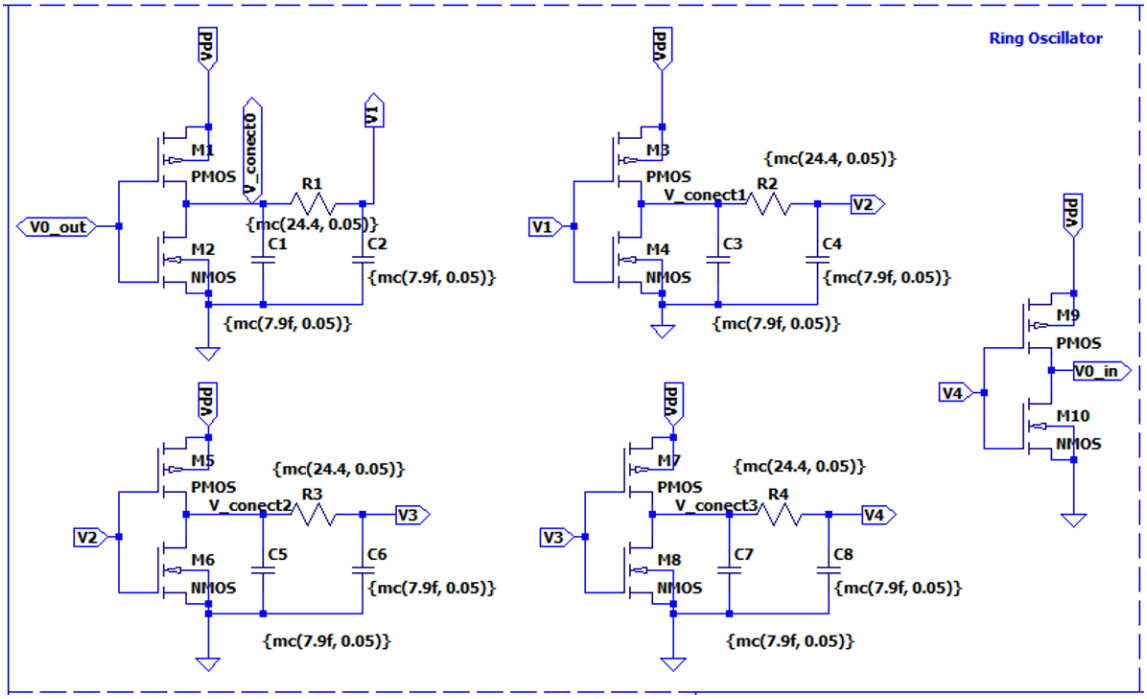


Figure 15: Failure Sentinels RO Core sub-circuit

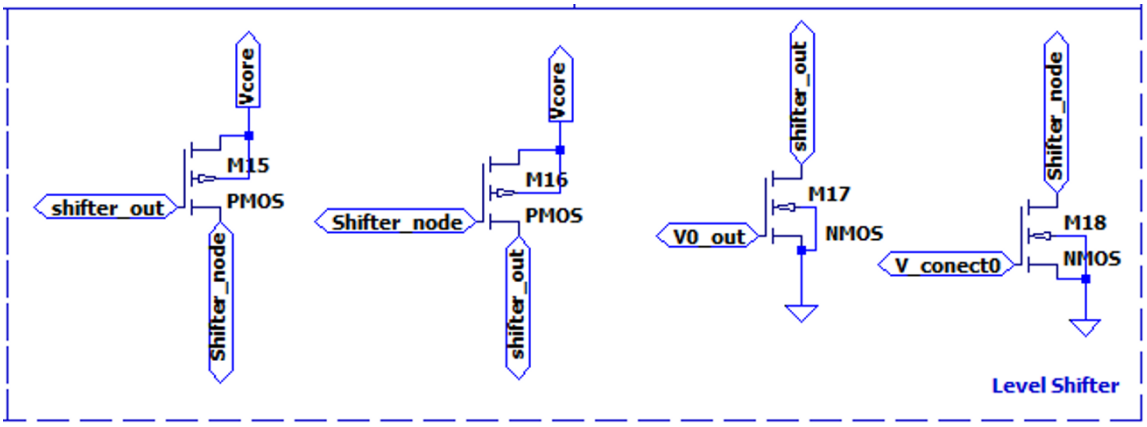


Figure 16: Failure Sentinels Level Shifter block

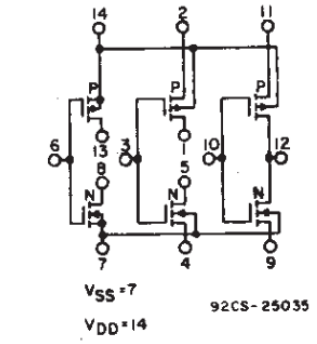


Figure 17: CD4007UB functional diagram
Texas Instruments, 2003 [25]

Table 1: CMOS comparison

Series	V_supply (V)
4000 [25]	3 to 18
74C [26]	3 to 15
74HC [27]	2 to 6
74HCT [28]	4.5 to 5.5
74LV [29]	1 to 3.6
74LVC [30]	1.2 to 3.6

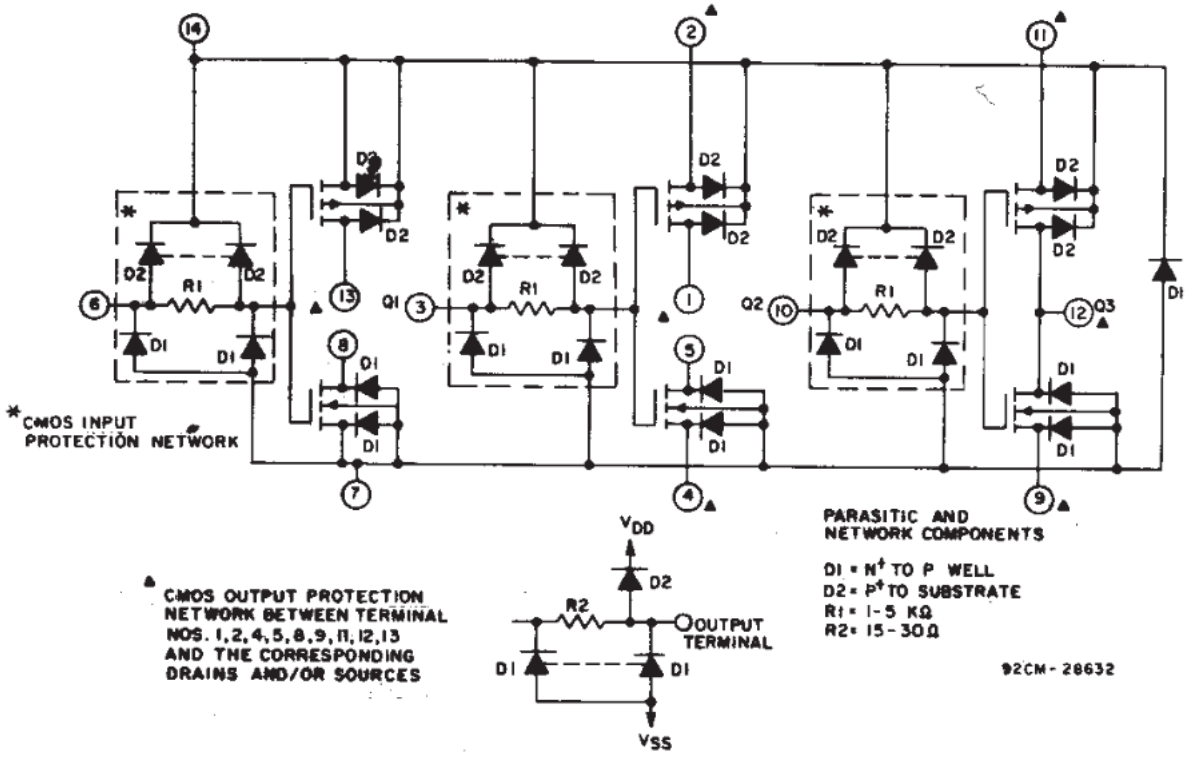


Figure 18: CD4007UB internal schematics
Texas Instruments, 2003 [25]

Those pieces of information indicate it is possible to implement the Failure Sentinels circuit through discrete CMOS components. However, their higher supply voltage, compared to the original one, leads to a strict oscillation measurement range caused by the Voltage Divider. This fact suggests not using that block, but it would change the original project, which is not our goal. Therefore, other options with lower voltage supply were considered, as shown in Table 1. Hence the lowest CMOS supply voltage found is 1v. It would be feasible with a system supply voltage from 3.0v to 3.6v, as the oscillation voltage is given by Equation 1. However, even those CMOS have their protection circuits that consume energy, which indicates an alternative approach was required.

Once using CMOS is not feasible, the natural idea was to use discrete NMOS and PMOS to operate as a CMOS. After researching several datasheets, our conclusion was to use Texas Instruments CSD13385F5 [31] and CSD23285F5 [32] because they have no direct connection to their substrate, which is a relevant feature to implement the NAND gate and is the primary restraint when choosing the devices to be used.

Figure 19 presents the discrete circuit Prototype 1 schematics, whose main differences from the original layout shown in Figure 10 are the NAND gate and the removal from the capacitance and resistances between components since discrete MOSFETs already have intrinsic resistance and capacitance values.

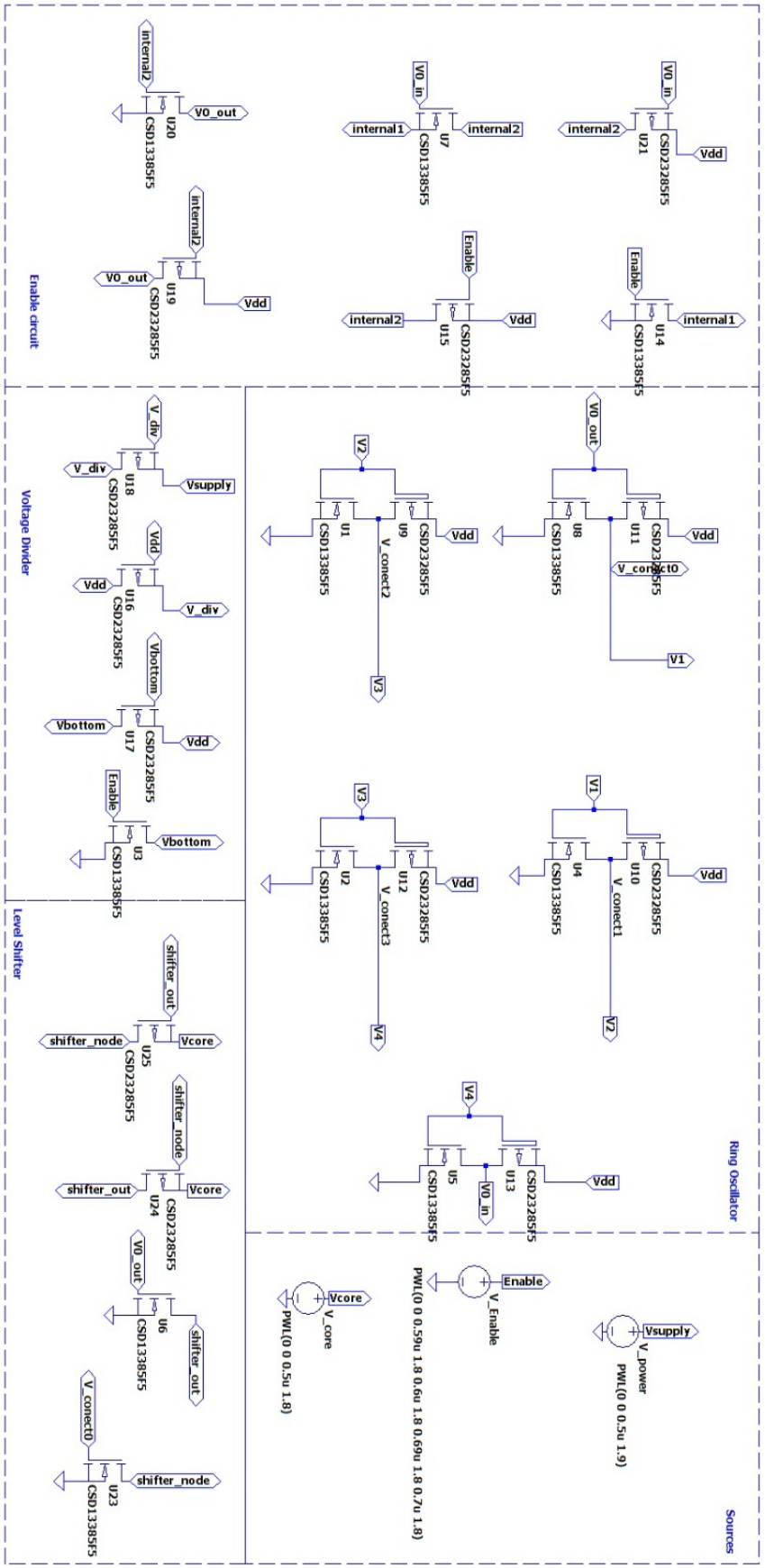


Figure 19: Prototype 1 schematics

4 Development

The discrete circuit simulation provided crucial results to the project's development. For instance, the discrete Level Shifter block generated a high transient for the whole RO circuit besides being unable to generate the expected output signal. Figure 20 illustrates how the output $shifter_{out}$ does not follow the input $V_{0_{in}}$, what would be the desired behavior.

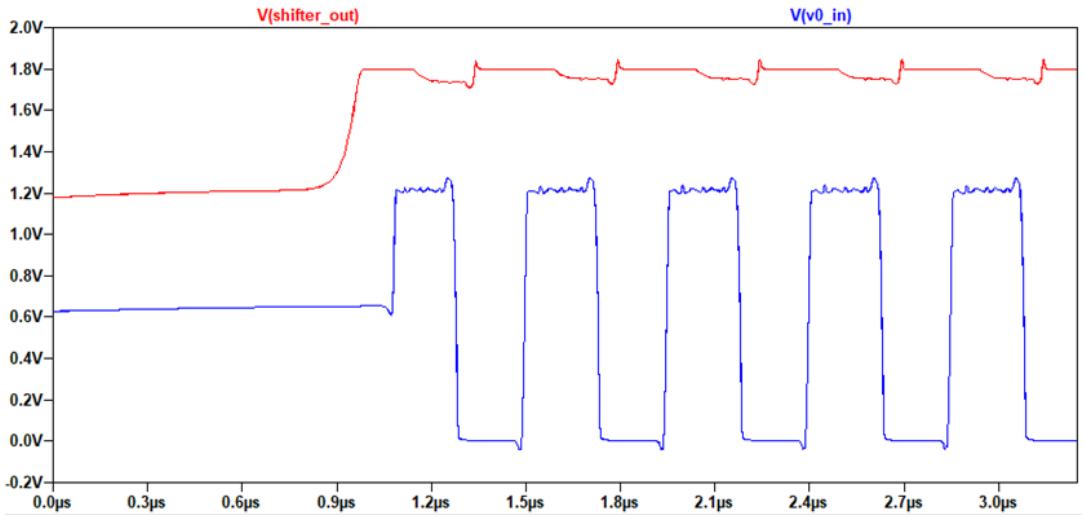


Figure 20: Level Shifter unexpected output

Analyzing the Level Shifter operation isolated from the rest of the circuit, we noted this module could not properly work due to the MOSFET V_{gs} value and the high signal transitions amount. We added a high resistance in MOSFETs gates to increase the internal input capacitor discharge time, but it was unsuccessful. Therefore, we conclude it is not possible to discretely implement this circuit similarly as it was lithographically designed by Xingyuan et al. [33] and Halak et al. [34] since the commercial FETs are not able to have such a low V_{gs} value nor a transition time short enough to shift these low voltages.

Hence the original topology is not feasible for discrete devices. We implemented two alternative layouts to generate an output signal that is sufficiently similar to the original Level Shifter output. These ideas are to use a single NMOS or CMOS model.

The idea of using a single NMOS model is to reduce the necessity of switching devices to improve output signal quality. The topology shown in Figure 21 is widely used in communications as I^2C and direct pin-to-pin GPIO connection [35] [36]. Its operation principle consists of keeping the potential difference in the NMOS gate at the lowest voltage level.

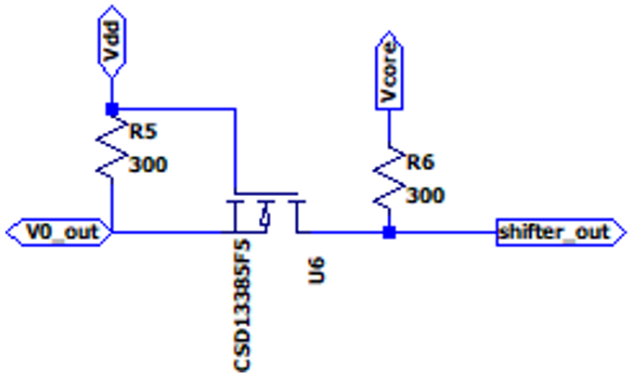


Figure 21: Level Shifter NMOS topology

If there is no signal from RO, the line voltage increases to the source voltage due to the pull-up resistor. Therefore the MOSFET threshold voltage $V_{gs_{th}}$ is under the limit, so the device does not conduct. Thus, the NMOS drain output has a pull-up resistor has a high voltage level. That way, both RO and output default

levels are high. When MOSFET conduces in the received RO signals for the negative part from $V_{gs_{th}}$ setting drain output as low, the output replicates the same variations in both high and low sides.

However, this topology has some features that must be considered as allowing bi-directional transmissions, which means the high-level output could operate as an input, which is undesired in our application. Besides, this layout is not usually deployed in low-voltage and high-frequency applications, so choosing and using components would be challenging. Finally, this circuit was designed so that the pull-up resistor values are defined for a single or very narrow reference value, decreasing the frequency range resolution.

The single CMOS topology shown in Figure 22 demands more supply voltage. NMOS connects the two signals from RO, which control the output, defined as the difference between two RO core subsequent stages.

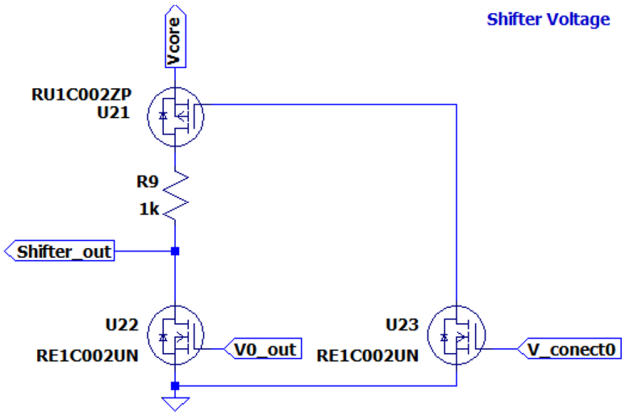


Figure 22: Level Shifter CMOS topology

The CMOS-based topology presented a better resolution in comparison to the NMOS-based. However, signal transitions are still problematic since they are related to V_{gs} and high-frequency values related to the CMOS output resistance. As this topology presented the best performance so far, we defined it as the Level Shifter circuit for our application.

Besides the Level Shifter, the Voltage Divider operation also differed from expected, as shown in Figure 23, in the original and the NMOS-PMOS-based circuit tests, as the resulting voltage was higher than Equation 1 estimates. This occurs because the NMOS would theoretically have an impedance considerably lower than PMOS's, which was not observed in the simulations, increasing the switching noise jitter energy loss and the output impedance. The high output impedance is a severe problem as the impedance seen by the divider is similar to that seen by the other modules. In a way, these blocks interfere with the Voltage Divider output voltage and consume unnecessary power.

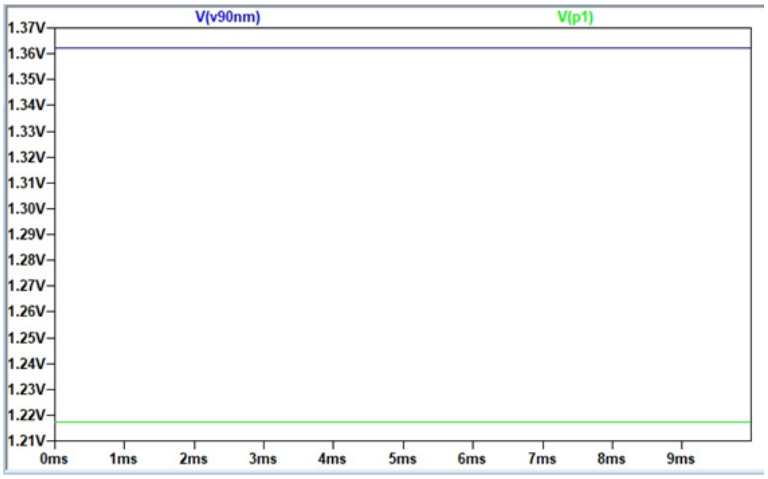


Figure 23: Voltage Divider operation

Analyzing all discussed problems, we concluded the original circuit would benefit from a more robust

treatment of the voltage level, but it would increase the energy consumption. Regarding the proposed topologies, the results are unsatisfying, which demonstrates a better topology is yet required.

Besides, these topologies analysis highlighted three relevant features when developing the following topology. First, achieving a satisfying response time trade-off is necessary, as capacitors and resistors interfere with the oscillation frequency besides the response time itself. Second, it must not intensely treat signal, as noise removal demands power. Third, its output must reflect the oscillation minimizing the switching noise jitter losses as low as possible.

Furthermore, Prototype 1 data were crucial to understanding which NMOS and PMOS features are more relevant when paired as CMOS in this application. For instance, RO CMOS must have strictly equal V_{gs} since this value is also necessary for frequency analysis. Similarly, their V_{th} must also be strictly equal and lower, maximizing the output frequency range.

Besides, the RO CMOS operation resistance $R_{DS_{on}}$, also known as MOSFET's output resistance, must be the closest as possible so the output current has a constant behavior to avoid changing its direction in transitions, and consequently, loses power. Also, regarding transitions, Rise, Fall, Turn-on, and Turn-off delay times must be extremely close to avoid short circuits in those moments, which could damage the hardware from the MOSFETs to the MCU.

Finally, input $C_{i_{SS}}$, output $C_{o_{SS}}$ and inverse transfer $C_{r_{SS}}$ capacitances besides the MOSFET's transconductance must also be considered, for its direct relation to the previously mentioned times. Actually, these parameters are mathematically related, which can be demonstrated using the NMOS high-frequency model presented in Figure 24 [23].

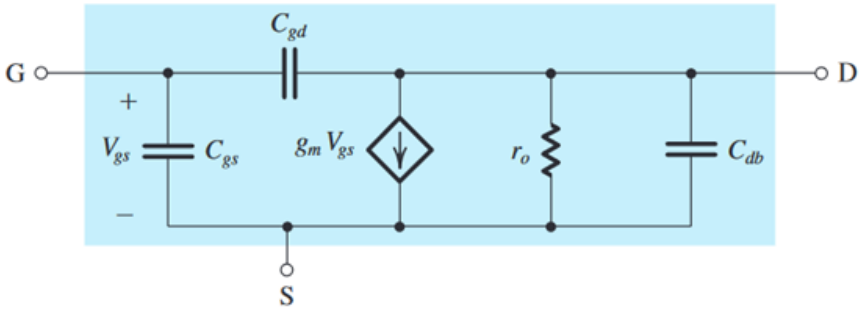


Figure 24: NMOS high-frequency model
Sedra et al. [23]

This model introduces the gate-source C_{gs}, gate-drain C_{gd} and drain-source C_{db} capacitances. Since these parameters are not present in datasheets, Equations 2, 3 and 4 presents their algebraic relations to $C_{i_{SS}}$, $C_{o_{SS}}$ and $C_{r_{SS}}$ [23].

$$C_{i_{SS}} = C_{gs} + C_{gd} \tag{2}$$

$$C_{o_{SS}} = C_{db} + C_{gd} \tag{3}$$

$$C_{r_{SS}} = C_{gd} \tag{4}$$

Finally, it is possible to conclude the algebraic relation between the mentioned internal capacitances, the transconductance, and the transition frequency with Equation 5 [23]. In our application, it is interesting to maximize the f_t parameter.

$$f_t = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{5}$$

Besides, Figure 25 illustrates how transconductance g_m can also be approximated as the relation described in Equation 6 between the drain current I_d, threshold voltage V_{th} and gate-source voltage V_{gs} [23].

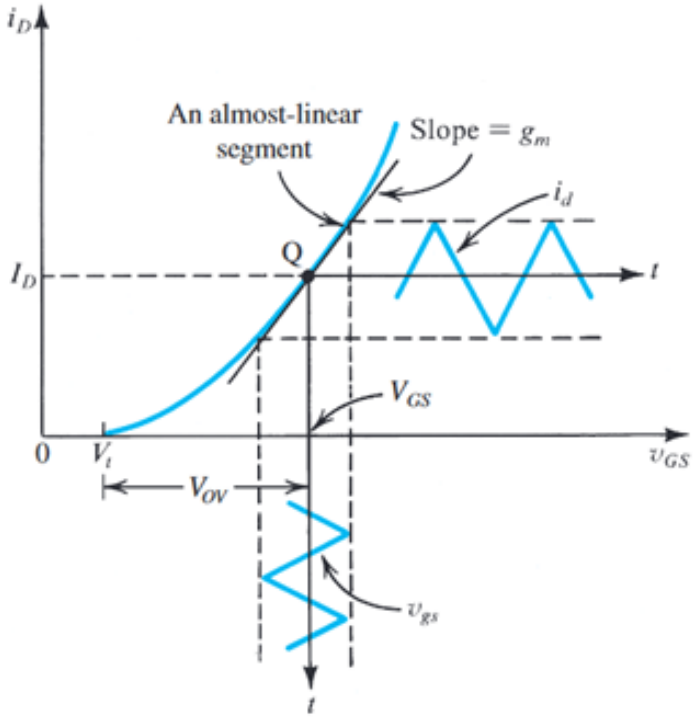


Figure 25: g_m approximation
Sedra et al. [23]

$$g_m = \frac{I_d}{V_{gs} - V_{th}} \tag{6}$$

After introducing these parameters, we can calculate their values in Prototype 1. Figure 4 shows g_m is 11.3 S for I_d 0.9 A in the CSD13385F5 NMOS datasheet [32].

$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.5	0.8	1.2	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 1.8 V, I_{DS} = 0.1 A		26	50	mΩ
		V_{GS} = 2.5 V, I_{DS} = 0.9 A		18	23	
		V_{GS} = 4.5 V, I_{DS} = 0.9 A		15	19	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_{DS} = 0.9 A		11.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		519	674	pF
C_{oss}	Output capacitance			305	396	pF
C_{rss}	Reverse transfer capacitance			29	38	pF
R_G	Series gate resistance			20		Ω

Figure 26: CSD13385F5 g_m
CSD13385F5 –12-V, N-Channel FemtoFET™ MOSFET [32]

Since the V_{ds} value relative to an 11.3 S transconductance is different from the value indicated for the capacitances in Figure 4, it is necessary to use the capacitance-voltage relation given in Figure 4.

From Figure 4, it is possible to estimate $C_{i_{SS}}$ and $C_{r_{SS}}$ as 550pF and 100pF, respectively, for a 1.2V_{ds}. Then, applying these values in Equation 5, the transition frequency is approximately 3.27MHz.

Repeating this procedure for CSD13385F5 PMOS, its datasheet, shown in Figure 4, which indicates an 8.9S transconductance g_m for a -1A drain current I_d [31].

Once again, it is necessary to use the capacitance-voltage relation shown in Figure 4, where it is possible

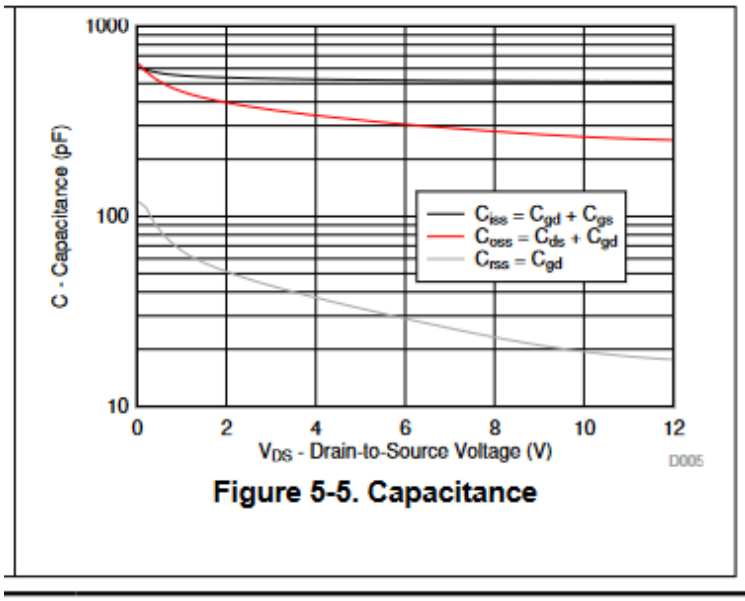


Figure 5-5. Capacitance

Figure 27: CSD13385F5 dynamic characteristics
CSD13385F5 –12-V, N-Channel FemtoFET™ MOSFET [32]

$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.40	–0.65	–0.95	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_{DS} = –1 A		64	130	mΩ
		V_{GS} = –1.8 V, I_{DS} = –1 A		49	80	
		V_{GS} = –2.5 V, I_{DS} = –1 A		38	47	
		V_{GS} = –4.5 V, I_{DS} = –1 A		29	35	
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_{DS} = –1 A		8.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		483	628	pF
C_{oss}	Output capacitance			305	397	pF
C_{rss}	Reverse transfer capacitance			37	48	pF
R_G	Series gate resistance			17		Ω

Figure 28: CSD23285F5 g_m
CSD23285F5 –12-V, P-Channel FemtoFET™ MOSFET [31]

to estimate C_{iSS} and C_{rSS} as 500pF and 85pF, respectively, for a -1.2V_{ds}. Then, applying these values in Equation 5, the transition frequency is approximately 2.83MHz.

Thereby the theoretical limit for the CMOS transition frequency is approximately 2.83MHz, which is noticeably higher than the 2.3MHz observed in the simulation. Considering the f_t parameter indicates the MOSFET's maximum oscillation frequency, the observed values must be lower than that due to physical characteristics. One of those features is the MOSFET switching waste heat, which is related to the frequency the device operates.

This waste heat is directly-dependant on the circuit's duty cycle, the drain-source reverse current protection, and the low-pass filter created by the gate resistance alongside C_{gs}, contributing to signal attenuation. Equation 7 [24] gives this low-pass filter cutoff frequency.

$$f_c = \frac{1}{2\pi R_G C_{gs}} \tag{7}$$

Using R_G values from CSD13385F5 and CSD23285F5 datasheets with the estimate C_{gs} from Figures 4 and 4, Equation 7 indicates 18kHz and 23kHz cutoff frequencies, respectively.

The presented behavior demonstrates a huge dependency between the oscillation frequency and the g_m, C_{iSS}, and V_{gs} values. Therefore, finding a MOSFET in which V_{gs} and V_{th} values as lowest as possible would

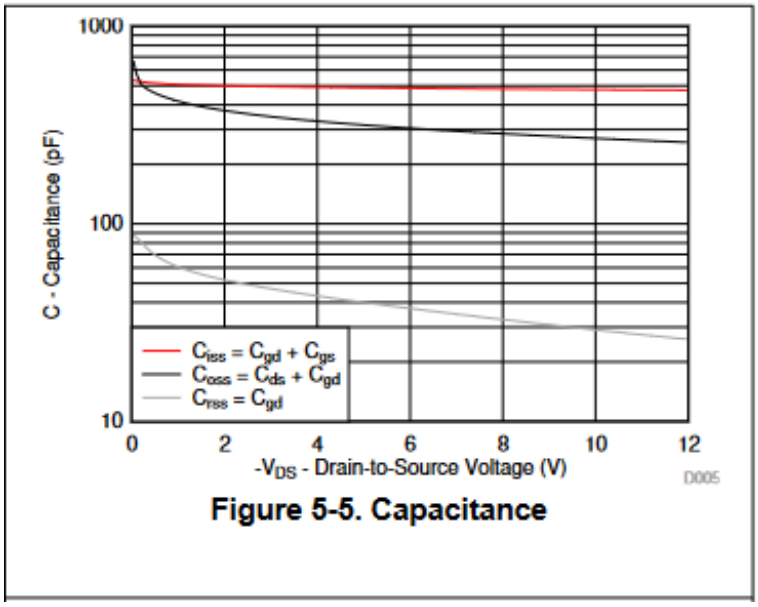


Figure 29: CSD23285F5 dynamic characteristics
CSD23285F5 –12-V, P-Channel FemtoFET™ MOSFET [32]

operate in low-frequency and low-voltage. Besides, as Figure 4 illustrates, the capacitances are inversely proportional to voltage, affecting the maximum transconductance setting.

From this better understanding of the MOSFETs parameters impact on this application, it is possible to design Prototype 2. Since the lowest $V_{gs(th)}$ value is desired, RE1C002UN [37] and RU1C002ZP [38] are the first candidates to implement the new circuit layout. Using their datasheet parameters for $1.2V_{ds}$ in Equation 5, the transition frequency is 7.23MHz and 5.68MHz, respectively.

These results demonstrate that only the $V_{gs(th)}$ value is insufficient to assure a high oscillation frequency since the capacitances, which have a relation curve with V_{ds}, also affect the transconductance. Besides, RE1C002UN and RU1C002ZP have a high R_{ds}, of approximately 1.2 Ω, which would be fantastic for the RO block but is not interesting for the Voltage Divider.

Thereby the Prototype 2 MOSFET must have low $V_{gs(th)}$ and R_{ds} values, which is the SI2342DS case **??**. This NMOS has 0.075Ω for a $1.2V_{ds}$, representing 16 times less than the previous pair. That way, using SI2342DS and RU1C002ZP as a CMOS pair would reduce the Voltage Divider block's output impedance and also reduce the NMOS resistor influence in the voltage divider. This is extremely required for it isolates the load influence on the output voltage, improving the output signal quality and resulting in better-defined levels on the oscillator's supply. Figure 30 presents the Prototype 2 schematic, which is built with SI2342DS and RU1C002ZP as a CMOS pair.

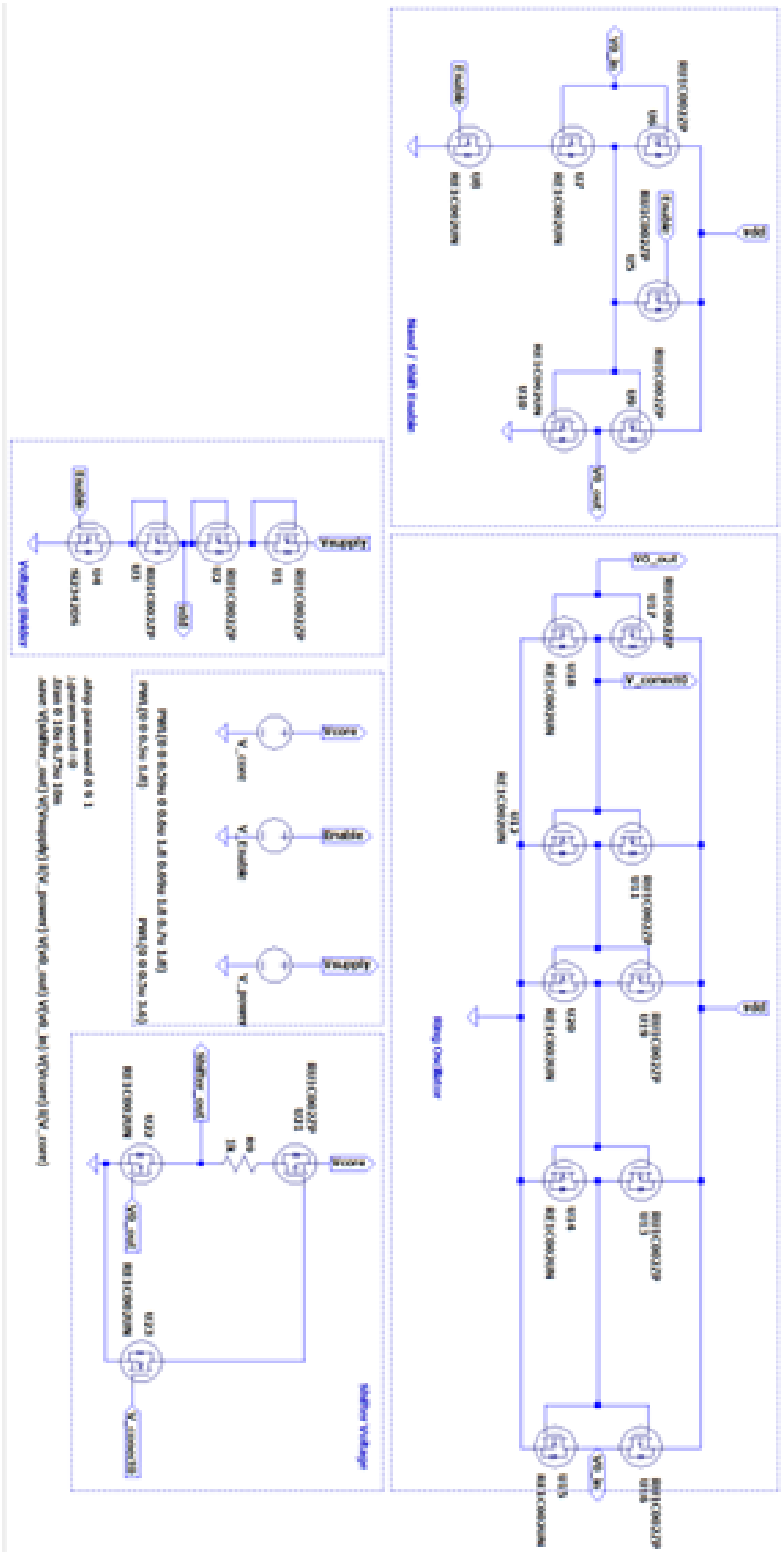
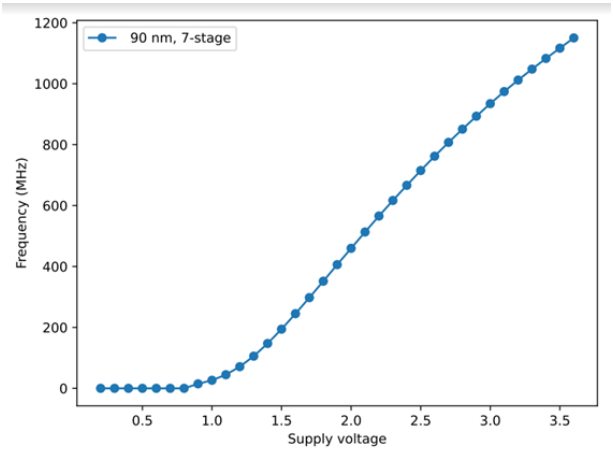


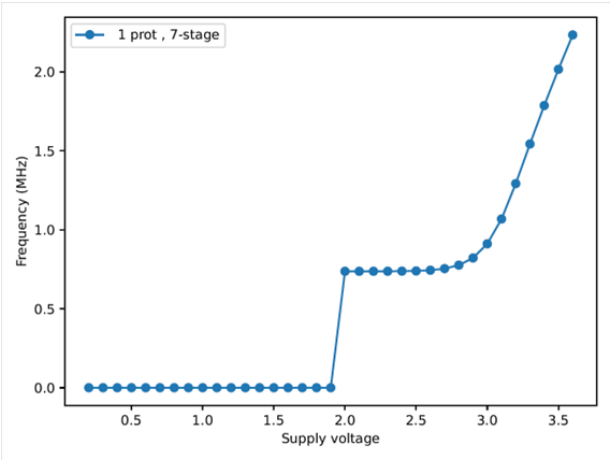
Figure 30: Prototype 2 schematics

5 Conclusions & future work

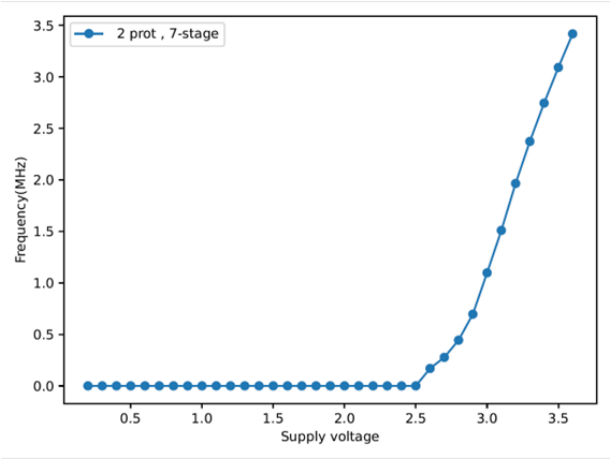
As explained in Section 3, we simulated 90nm 7-staged Failure Sentinels, Prototype 1 and Prototype 2 operation from 0.2v to 3.6v with 0.1v steps in LTspice to measure their RO frequency and power consumption, as we want to understand the circuit manufacturing impact in those parameters. Figure 31 presents each circuit RO frequency.



(a) 90nm 7-staged Failure Sentinels



(b) Prototype 1



(c) Prototype 2

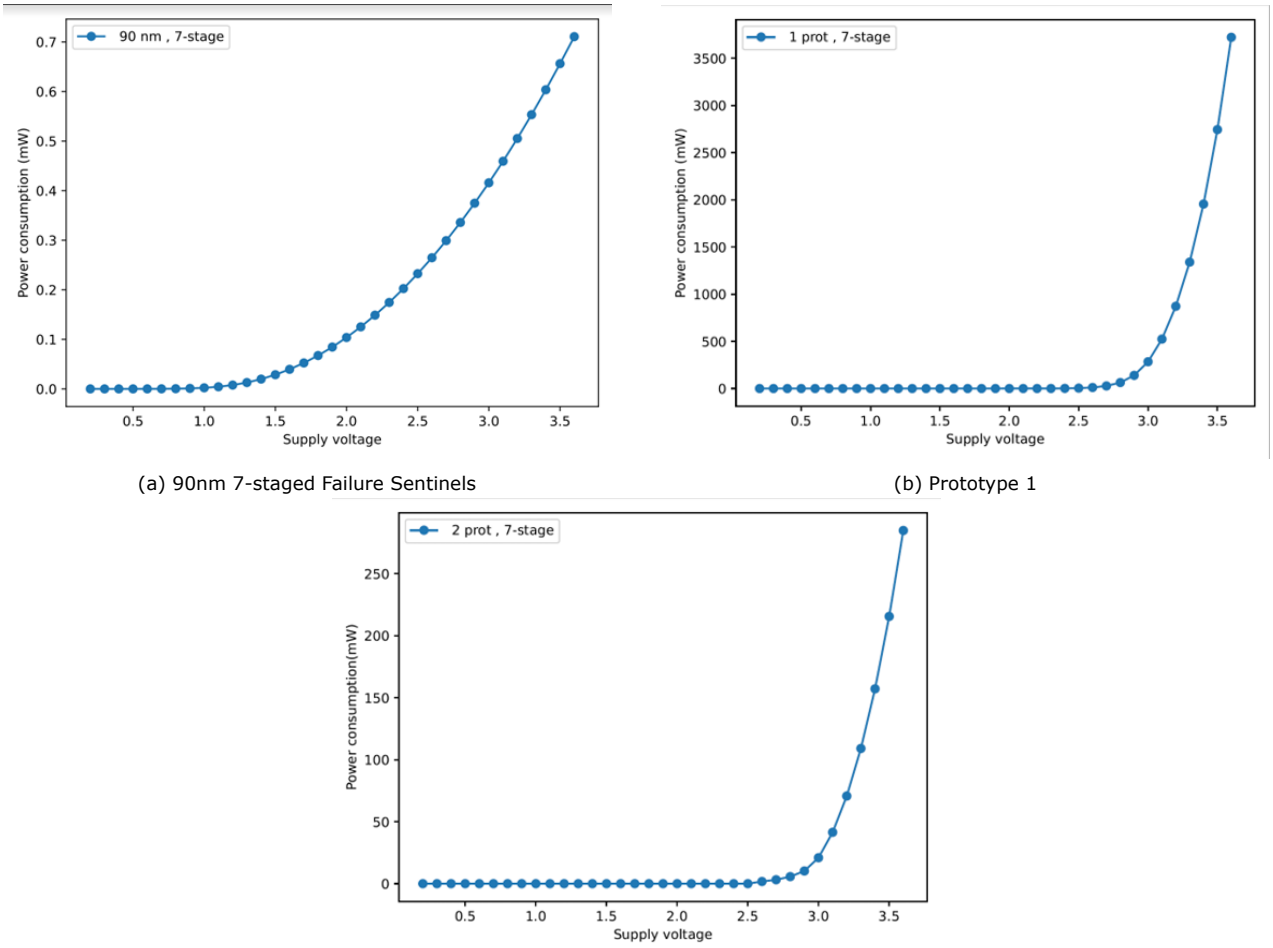
Figure 31: RO Frequency x Supply Voltage

Figure 31 confirms the lithographic design is far superior to the discrete one since the Subfigure 31a is almost linear for a wide voltage range, which is very interesting when converting the oscillation frequency into voltage measurement. The naive replacement of the lithographic CMOS for the NMOS-PMOS complementary pair did not present the desired behavior, as discussed in Section 4 and shown in Subfigure 31b. Finally, Prototype 2 also presented an almost linear behavior for the target voltage range, as illustrated by Subfigure 31c, but for a considerably smaller voltage range than 90nm 7-staged Failure Sentinels and in substantially lower frequencies.

Similarly, Figure 32 presents the circuits' power consumption. Subfigure 32a demonstrates how the lithographic design is unarguably more efficient than the discrete approach. Furthermore, Subfigure 32c confirms $V_{gs(th)}$ and R_{ds} are relevant to the NMOS-PMOS complementary pair consumption since it is more than ten times lower than the Prototype 1 naive approach presented by Subfigure 32b.

Based on the simulation results, presented in Figures 31 and 32, and the theory about MOSFETs, it can be stated that the use of discrete circuits for the VCO model presented by the Failure Sentinels work is unlikely to be fully implemented using the currently available discrete components in the market, especially for lower voltage values.

This is due to the characteristic of commercial MOSFETs that operate with a voltage threshold $V_{gs(th)}$ around



(a) 90nm 7-staged Failure Sentinels

(b) Prototype 1

(c) Prototype 2

Figure 32: Power consumption

0.3v to 0.6v for the transition point between the triode region and the active operating region (saturation), while the minimum voltage between the drain and source V_{ds} for these components is approximately twice the $V_{gs(th)}$, so their operating range would be between 0.6v and 1.2v.

With the CMOS power supply range limited to 1/3 of the EH generation, we find that the minimum voltage for the operation of this device is between 1.8v and 3.6v. This means that even using the best commercial MOSFETs, the smallest possible conversion value would be 1.8v, which is approximately half of the proposed maximum resolution. This represents a considerably narrower range than the lithography proposed, as confirmed by the experiment.

Nevertheless, this research allowed a further understanding and comprehension regarding commercial MOSFET features that help in oscillator applications, which are not exclusively for EH purposes. For instance, VCOs can also be used in frequency synthesis, modulation, PLL, and programable oscillators, besides phase-control circuits.

This research identified promising paths for developing discrete VCOs in Energy Harvesting applications, such as module revisions, utilizing low-power modules, comparison with low-power oscillator modules, and real assembly.

Modifying specific modules, such as removing the voltage divider, allows for the use of higher values of $V_{gs(th)}$, resulting in selecting a more suitable operating point for the MOSFET. Furthermore, it enables implementation with CMOS chips and logic circuits. On the other hand, utilizing low-power modules, such as the IC TRANSLTR UNIDIRECTIONAL, can be a viable solution for the level shifter, reducing the overall circuit power consumption.

It is essential to compare with low-power oscillator modules available in the market since it is possible

some built-in devices would perform as expected from one of the Failure Sentinels blocks. Additionally, it is essential to perform the actual circuit assembly, either through lithography, if possible, or by using a discrete model. This step is crucial to validate the values obtained from the simulations since factors such as thermal variations and parasitic losses are not accurately modeled in simulators. Besides, replicating an Energy Harvesting profile in LTspice may not reproduce the real-life behavior.

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