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Anexo 1 - Condições de Contorno guia NRD

Equações de propagação no meio dielétrico homogêneo sem fontes e sem cargas:

Equações de Maxwell na forma diferencial (pontual):

1) $\nabla \cdot \vec{D} = 0$ [Lei de Gauss campo elétrico para um meio (volume) sem fonte]

2) $\nabla \cdot \vec{B} = 0$ [Lei de Gauss para campo Magnético]

3) $\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} = -j\omega\mu \vec{H}$ [Lei de Faraday]

4) $\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} = \sigma \vec{E} + j\omega\varepsilon_c \vec{E}$ [Lei de Ampére]

$$\nabla \times \vec{H} = \left[(\sigma + \omega\varepsilon'') + j\omega\varepsilon'\right]\vec{E}$$

Relações constitutivas do meio:

$$\vec{D} = \varepsilon \vec{E} \qquad \vec{B} = \mu \vec{H} \qquad \vec{J} = \sigma \vec{E}$$

A permissividade complexa do meio dielétrico é :

$$\varepsilon_c = \varepsilon' - j\varepsilon''$$

$$\varepsilon' = \varepsilon_{eff}$$

sendo ε'' referente as perdas de polarização

A condutividade efetiva do meio é :

$$\sigma_{ef} = \sigma + \omega\varepsilon''$$

Equação de onda vetorial para o campo elétrico

$$\nabla^2 \vec{E} + k^2 \vec{E} = 0$$

$$\nabla^2 \vec{E} - j\omega\mu\left[(\sigma + \omega\varepsilon'') + j\omega\varepsilon'\right]\vec{E} = 0$$

Equação de onda vetorial para o campo Magnético.

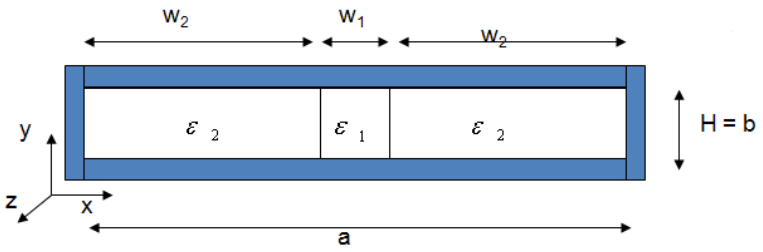
$$\nabla^2 \vec{H} + k^2 \vec{H} = 0$$

$$\nabla^2 \vec{H} - j\omega\mu\left[\left(\sigma + \omega\varepsilon^{''}\right) + j\omega\varepsilon^{'}\right]\vec{H} = 0$$

A partir das equações de onda vetorial para o campo elétrico e magnético obtém

$$k^2 = -j\omega\mu\left[\left(\sigma + \omega\varepsilon^{''}\right) + j\omega\varepsilon^{'}\right]$$

Condições de Contorno em um guia dielétrico formado por 2 meios dielétricos sem fontes e sem cargas de paredes metálicas:



1ª) considerando a superfície das Paredes metálicas:

1.A) Na parede superior (y=b) as componentes tangenciais do campo elétrico são nulas, isto é $E_x = 0 = E_z$ reescrevendo:

E_{x1} ($w_2 < x < a- [w_{2\,+}\, w_1]$; y=b ; z) = E_{x2} ($w_2 + w_1 < x < a$; y=b ; z) = E_{x2} ($0< x <w_2$; y=b ; z) = 0

E_{z1} ($w_2 < x < a- [w_2 + w_1]$; y=b ; z) = E_{z2} ($w_2 + w_1 < x < a$; y=b ; z) = E_{z2} ($0< x <w_2$; y=b ; z) = 0

1.B) Na parede inferior (y=0) as componentes tangenciais do campo elétrico são nulas, isto é $E_x = 0 = E_z$, reescrevendo :

E_{x1} ($w_2 < x < a- [w_2 + w_1]$; y=0 ; z) = E_{x2} ($w_2 + w_1 < x < a$; y=0 ; z) = E_{x2} ($0< x <w_2$; y=0 ; z) = 0

E_{z1} ($w_2 < x < a- [w_2 + w_1]$; y=0 ; z) = E_{z2} ($w_2 + w_1 < x < a$; y=0 ; z) = E_{z2} (0< x <w_2 ; y=0 ; z) = 0

1.C) Na parede esquerda (x=0) as componentes tangenciais do campo elétrico são nulas, isto é, $E_z = 0 = E_y$, reescrevendo:

E_{y2} (x=0 ; 0<y <b ; z) = E_{z2} (x=0 ; 0 < y < b ; z) = 0

1.D) Na parede da direita (x =a) as componentes tangenciais do campo elétrico são nulas, isto é $E_z = 0 = E_y$, reescrevendo :

E_{y2} (x=a ; 0<y <b ; z) = E_{z2} (x=a ; 0 < y < b ; z) = 0

2ª) Considerando a superfície de separação entre os dois meios dielétricos:

2.A) Continuidade do campo elétrico tangencial e campo magnético tangencial, isto é, em x= w_2 , $E_{y1} = E_{y2}$ e $H_{y1} = H_{y2}$ assim como $E_{z1} = E_{z2}$ e $H_{z1} = H_{z2}$, reescrevendo :

E_{y1}(x=w_2 ; 0< y <b ; z) = E_{y2} (x=w_2 ; 0< y <b ; z)
H_{y1} (x=w2 ; 0< y <b ; z) = H_{y2} (x=w2 ; 0< y <b ; z)
E_{z1}(x=w_2 ; 0< y <b ; z) = E_{z2} (x=w_2 ; 0< y <b ; z)
H_{z1} (x=w_2 ; 0< y <b ; z) = H_{z2} (x=w_2 ; 0< y <b ; z)

2.B) Continuidade do campo elétrico tangencial e campo magnético tangencial, isto é, em x= a-(w_2+w_1) , $E_{y1} = E_{y2}$ e $H_{y1} = H_{y2}$ assim como $E_{z1} = E_{z2}$ e $H_{z1} = H_{z2}$, reescrevendo :

E_{y1}(x= a-(w_2+w_1) ; 0< y <b ; z) = E_{y2} (x= a-(w_2+w_1) ; 0< y <b ; z)
H_{y1} (x= a-(w_2+w_1) ; 0< y <b ; z) = H_{y2} (x= a-(w_2+w_1) ; 0< y <b ; z)
E_{z1}(x= a-(w_2+w_1) ; 0< y <b ; z) = E_{z2} (x= a-(w_2+w_1) ; 0< y <b ; z)
H_{z1} (x= a-(w_2+w_1) ; 0< y <b ; z) = H_{z2} (x= a-(w_2+w_1) ; 0< y <b ; z)

A) Modos de propagação LSEx (Longitudinal Section Electric) ou TEx (Transversal Electric) em relação a x :

$\vec{B} = \mu \vec{H}$ $\vec{J} = \sigma \vec{E}$

$$\nabla \cdot \vec{D} = 0 \qquad \nabla \cdot \vec{B} = 0$$

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} = -j\omega\mu \vec{H} \qquad \nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} = \vec{J} + j\omega\varepsilon \vec{E}$$

Solução aplicando o potencial vetor (F) para o campo elétrico num meio homogêneo sem fontes e sem correntes magnéticas

$$\nabla \cdot \vec{D} = 0 = \nabla \cdot \varepsilon \vec{E} \qquad \vec{E} = -\frac{1}{\varepsilon} \nabla \times \vec{F} \qquad \vec{H} = -\frac{\nabla \times \vec{E}}{j\omega\mu}$$

Objetivo encontrar a solução para a equação de onda do vetor potencial elétrico que satisfaça as condições de contorno

$$\nabla^2 \vec{F} + k^2 \vec{F} = 0$$

Considerando a propagação na direção z^+ , como nos modos TE^x em relação a x a componente na direção x do campo elétrico é zero ($E_x = 0$) desta forma ao resolver o rotacional de F, o potencial elétrico F só terá a direção x , variando em x, y, z sendo uma combinação linear de 3 soluções isto é:

$$F_x(x, y, z) = f(x) \cdot g(y) \cdot h(z) = [C_1 \cos(\beta_x x) + D_1 sen(\beta_x x)] \cdot [C_2 \cos(\beta_y y) + D_2 sen(\beta_y y)] \cdot [C_3 e^{-j\beta_z z}]$$

Equações do campo elétrico e campo magnético:

$$E_x = 0 \qquad H_x = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 F_x}{\partial x^2} + k^2 F_x\right]$$

$$E_y = -\frac{1}{\varepsilon}\frac{\partial F_x}{\partial z} \qquad H_y = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 F_x}{\partial x \partial y}\right]$$

$$E_z = \frac{1}{\varepsilon}\frac{\partial F_x}{\partial y} \qquad H_z = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 F_x}{\partial x \partial z}\right]$$

$$\vec{E} = E_x \cdot \hat{a}_x + E_y \cdot \hat{a}_y + E_z \cdot \hat{a}_z$$

$$\vec{H} = H_x \cdot \hat{a}_x + H_y \cdot \hat{a}_y + H_z \cdot \hat{a}_z$$

$$k^2 = \beta_x^2 + \beta_y^2 + \beta_z^2 = \omega^2 \mu\varepsilon$$

Equações do campo elétrico e campo magnético nos meios dielétricos 1 e 2 : $\beta_{x2}, \beta_{x1}, \beta_{y2}, \beta_{y1}, \beta_{z2}, \beta_{z1}$

Meio 1	Meio 2	Meio 1	Meio 2
$E_{x1} = 0$	$E_{x2} = 0$	$H_{x1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 F_{x1}}{\partial x^2} + k^2 F_{x1}\right]$	$H_{x2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 F_{x2}}{\partial x^2} + k^2 F_{x2}\right]$
$E_{y1} = -\frac{1}{\varepsilon_1}\frac{\partial F_{x1}}{\partial z}$	$E_{y2} = -\frac{1}{\varepsilon_2}\frac{\partial F_{x2}}{\partial z}$	$H_{y1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 F_{x1}}{\partial x \partial y}\right]$	$H_{y2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 F_{x2}}{\partial x \partial y}\right]$
$E_{z1} = \frac{1}{\varepsilon_1}\frac{\partial F_{x1}}{\partial y}$	$E_{z2} = \frac{1}{\varepsilon_2}\frac{\partial F_{x2}}{\partial y}$	$H_{z1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 F_{x1}}{\partial x \partial z}\right]$	$H_{z2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 F_{x2}}{\partial x \partial z}\right]$

Aplicando as condições de contorno para os meios 1 e 2 em função das relações equivalência de H_1, E_1 , H_2, E_2 nas paredes superiores e inferiores , assim como nas superfícies de separação entre os meios, obtém:

$$F_x(x,y,z)=[D_1 sen(\beta_x x)]\cdot[C_2\cos(\beta_y y)]\cdot[C_3 e^{-j\beta_z z}]$$

$$F_{x1}(x,y,z)=[D_{11} sen(\beta_{x1} x)]\cdot[C_{21}\cos(\beta_{y1} y)]\cdot[C_{31} e^{-j\beta_{z1} z}]$$

$$F_{x2}(x,y,z)=[D_{12} sen(\beta_{x2} x)]\cdot[C_{22}\cos(\beta_{y1} y)]\cdot[C_{32} e^{-j\beta_{z2} z}]$$

Obtém :

$$\beta_{y1}=\beta_{y2}=\frac{n\pi}{b}$$

$$\beta_{z1}=\beta_z$$

$$\beta_{z2}=0$$

$$k_1^2=\beta_{x1}^2+\beta_{y1}^2+\beta_{z1}^2=\omega^2\mu_1\varepsilon_1$$

$$k_2^2=\beta_{x2}^2+\beta_{y2}^2+\beta_{z2}^2=\omega^2\mu_2\varepsilon_2$$

$LSE^x_{m,n}$

$$\frac{\beta_{x1}}{\mu_1}\cot(\beta_{x1}\cdot(a-(w_2+w_1))=\frac{\beta_{x2}}{\mu_2}\cot(\beta_{x2}\cdot(w_2))$$

A freqüência de corte para os modos $TE^x_{m,0}$ ou $LSE^x_{m,0}$

$$\frac{\sqrt{\mu_1\varepsilon_1}}{\mu_1}\cot\left(\omega_c\sqrt{\mu_1\varepsilon_1}\cdot(a-(w_2+w_1)\right)=\frac{\sqrt{\mu_2\varepsilon_2}}{\mu_2}\cot\left(\omega_c\sqrt{\mu_2\varepsilon_2}\cdot(w_2)\right)$$

A freqüência de corte para os modos $TE^x_{0,1}$ ou $LSE^x_{0,1}$

$$\frac{1}{2b\sqrt{\mu_2\varepsilon_2}}>f_c(TE^x_{0,1})>\frac{1}{2b\sqrt{\mu_1\varepsilon_1}}$$ Sendo $\mu_2\varepsilon_2<\mu_1\varepsilon_1$

B) Modos de propagação LSMx (Longitudinal Section Magnetic) ou TMx (Transversal Magnetic) em relação a x :

$$\vec{J}=\sigma\vec{E}$$

$$\vec{B}=\mu\vec{H}$$

$$\vec{D}=\varepsilon\vec{E}$$

$$\nabla\cdot\vec{D}=0$$

$$\nabla\cdot\vec{B}=0$$

$$\nabla\times\vec{E}=-\frac{\partial\vec{B}}{\partial t}=-j\omega\mu\vec{H}$$

$$\nabla\times\vec{H}=\vec{J}+\frac{\partial\vec{D}}{\partial t}=\vec{J}+j\omega\varepsilon\vec{E}$$

Solução aplicando o potencial vetor (A) para o campo magnético num meio homogêneo sem fontes e sem correntes magnéticas

$$\nabla\cdot\vec{B}=0=\nabla\cdot\mu\vec{H}$$

$$\vec{H}=\frac{1}{\mu}\nabla\times\vec{A}$$

$$\vec{E}=\frac{\nabla\times\vec{H}}{j\omega\varepsilon}$$

Objetivo encontrar a solução para a equação de onda do vetor potencial magnético que satisfaça as condições de contorno:

$$\nabla^2\vec{A}+k^2\vec{A}=0$$

Considerando a propagação na direção z^+ , como nos modos TM^x em relação a x a componente na direção x do campo magnético é zero ($H_x = 0$) desta forma ao resolver o rotacional de A, o potencial magnético A só terá a direção x , variando em x, y, z sendo uma combinação linear de 3 soluções isto é:

$$A_x(x,y,z) = f(x)\cdot g(y)\cdot h(z) = [C_1\cos(\beta_x x) + D_1 sen(\beta_x x)]\cdot[C_2\cos(\beta_y y) + D_2 sen(\beta_y y)]\cdot[C_3 e^{-j\beta_z z}]$$

Equações do campo elétrico e campo magnético:

$$H_x = 0 \qquad E_x = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 A_x}{\partial x^2} + k^2 A_x\right]$$

$$H_y = \frac{1}{\mu}\frac{\partial A_x}{\partial z} \qquad E_y = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 A_x}{\partial x \partial y}\right]$$

$$H_z = -\frac{1}{\mu}\frac{\partial A_x}{\partial y} \qquad E_z = \frac{1}{j\omega\mu\varepsilon}\left[\frac{\partial^2 A_x}{\partial x \partial z}\right]$$

$$\vec{E} = E_x\cdot\hat{a}_x + E_y\cdot\hat{a}_y + E_z\cdot\hat{a}_z$$

$$\vec{H} = H_x\cdot\hat{a}_x + H_y\cdot\hat{a}_y + H_z\cdot\hat{a}_z$$

$$k^2 = \beta_x^2 + \beta_y^2 + \beta_z^2 = \omega^2\mu\varepsilon$$

Equações do campo elétrico e campo magnético nos meios dielétricos 1 e 2 : $\beta_{x2}, \beta_{x1}, \beta_{y2}, \beta_{y1}, \beta_{z2}, \beta_{z1}$

$H_{x1} = 0$	$H_{x2} = 0$	$E_{x1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 A_{x1}}{\partial x^2} + k^2 A_{x1}\right]$	$E_{x2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 A_{x2}}{\partial x^2} + k^2 A_{x2}\right]$
$H_{y1} = \frac{1}{\mu_1}\frac{\partial A_{x1}}{\partial z}$	$H_{y2} = \frac{1}{\mu_2}\frac{\partial A_{x2}}{\partial z}$	$E_{y1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 A_{x1}}{\partial x \partial y}\right]$	$E_{y2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 A_{x2}}{\partial x \partial y}\right]$
$H_{z1} = -\frac{1}{\mu_1}\frac{\partial A_{x1}}{\partial y}$	$H_{z2} = -\frac{1}{\mu_2}\frac{\partial A_{x2}}{\partial y}$	$E_{z1} = \frac{1}{j\omega\mu_1\varepsilon_1}\left[\frac{\partial^2 A_{x1}}{\partial x \partial z}\right]$	$E_{z2} = \frac{1}{j\omega\mu_2\varepsilon_2}\left[\frac{\partial^2 A_{x2}}{\partial x \partial z}\right]$

Aplicando as condições de contorno para os meios 1 e 2 em função das relações equivalência de H_1, E_1 , H_2, E_2 nas paredes superiores e inferiores , assim como nas superfícies de separação entre os meios, obtém:

$$A_x(x,y,z)=[C_1\cos(\beta_x x)]\cdot[D_2 sen(\beta_y y)]\cdot[C_3 e^{-j\beta_z z}]$$

$$A_{x1}(x,y,z)=[C_{11}\cos(\beta_{x1} x)]\cdot[D_{21} sen(\beta_{y1} y)]\cdot[C_{31} e^{-j\beta_{z1} z}]$$

$$A_{x2}(x,y,z)=[C_{12}\cos(\beta_{x2} x)]\cdot[D_{22} sen(\beta_{y2} y)]\cdot[C_{32} e^{-j\beta_{z2} z}]$$

Obtém :

$$\beta_{y1}=\beta_{y2}=\frac{n\pi}{b}$$

$$\beta_{z1}=\beta_z$$

$$\beta_{z2}=0$$

$$k_1^2=\beta_{x1}^2+\beta_{y1}^2+\beta_{z1}^2=\omega^2\mu_1\varepsilon_1$$

$$k_2^2=\beta_{x2}^2+\beta_{y2}^2+\beta_{z2}^2=\omega^2\mu_2\varepsilon_2$$

$LSM^x_{m,n}$

$$\frac{\varepsilon_1}{\beta_{x1}}\cot(\beta_{x1}\cdot(a-(w_2+w_1))=\frac{\varepsilon_2}{\beta_{x2}}\cot(\beta_{x2}\cdot(w_2))$$

A freqüência de corte para os modos $TM^x_{m,0}$ ou $LSM^x_{m,0}$

$$\frac{\varepsilon_1}{\sqrt{\mu_1\varepsilon_1}}\cot\left(\omega_c\sqrt{\mu_1\varepsilon_1}\cdot(a-(w_2+w_1))\right)=\frac{\varepsilon_2}{\sqrt{\mu_2\varepsilon_2}}\cot\left(\omega_c\sqrt{\mu_2\varepsilon_2}\cdot(w_2)\right)$$

A freqüência de corte para os modos $TM^x_{0,1}$ ou $LSM^x_{0,1}$

$$\frac{1}{2b\sqrt{\mu_2\varepsilon_2}}>f_c\left(TM^x_{0,1}\right)>\frac{1}{2b\sqrt{\mu_1\varepsilon_1}}$$ Sendo $\mu_2\varepsilon_2<\mu_1\varepsilon_1$

Anexo 2 - Teorema de Floquet

Harmônicos espaciais (EBG = Electromagnetic Band Gap)

$$\beta_n = \frac{2n\pi}{d}$$

Floquet - Teorema básico para propagação de ondas em estruturas periódicas infinitas.

Harmônicos espaciais = cada termo da expansão da série de Fourier = fase

$$E(x,y,z) = \sum_{n=-\infty}^{\infty} f(x,y)e^{-j\left(\beta_z + \frac{2n\pi}{d}\right)z}$$

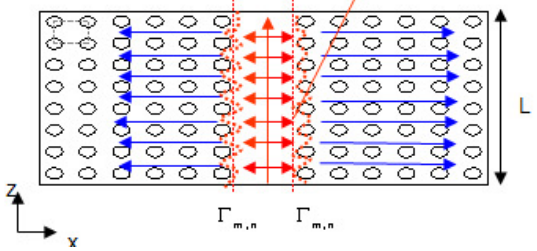
EBG - São os autovalores da matriz de transmissão $[T_{21}] \Leftrightarrow \beta_z$

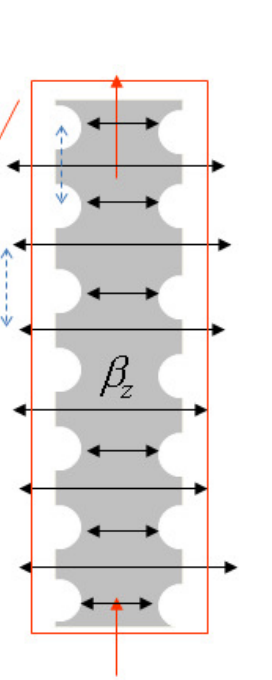
$$H(x,y,z) = \sum_{n=-\infty}^{\infty} g(x,y)e^{-j\left(\beta_z + \frac{2n\pi}{d}\right)z}$$

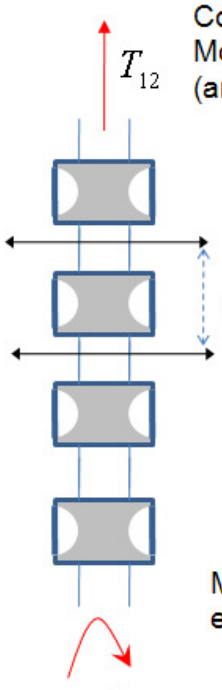
Solução não analítica = solução numérica

o caso deste guia dielétrico
gado, a constante de
agação é periódica num
alo d, gerando regiões
s de freqüências) de banda
ante e regiões proibidas).

ema : Definir a parede do
para obter dimensões deste
para ter uma solução
tica.







Coeficiente de transmissão
Modos transmitidos
(amplitude e fase)

$$\begin{bmatrix} c_1 \\ b_1 \\ \cdot \\ \cdot \\ \cdot \\ k_1 \end{bmatrix} = [T_{21}] \cdot \begin{bmatrix} c_2 \\ b_2 \\ \cdot \\ \cdot \\ \cdot \\ k_2 \end{bmatrix}$$

Modos incidentes (amplitude e fase)

Incidência de modos
TE ou TM

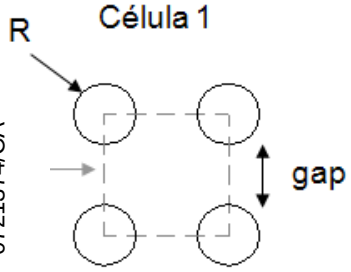
Coeficiente de reflexão
Modos refletidos

Anexo 3 - Diferentes configurações das vias do guia NRD

Aproximação da constante dielétrica ε_2

Diferentes configurações periódicas possíveis de vias:

Célula 1

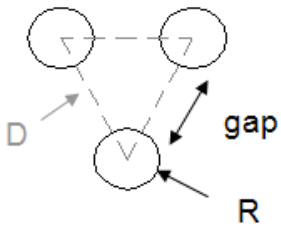


$$A_{celula} = D^2$$

$$A_{via} = \pi \cdot R^2$$

ou

Célula 2

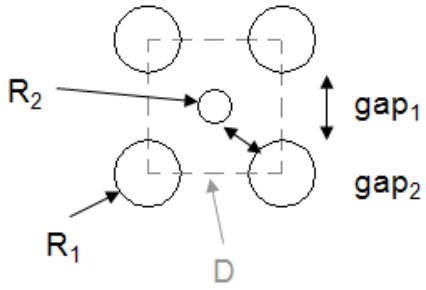


$$A_{celula} = \frac{D^2 \cdot \sqrt{3}}{4}$$

$$A_{via} = \pi \cdot R^2$$

ou

Célula 3



$$A_{celula} = D^2$$

$$A_{via} = \pi \cdot \left(R_1^2 + R_2^2\right)$$

$$\varepsilon_2 = \frac{\varepsilon_1 \cdot \left(A_{celula} - A_{via}\right) + A_{via}}{A_{celula}}$$

Anexo 4 - Dimensões do guia NRD

No guia carregado com 2 meios dielétricos obtém-se a freqüência de corte para os modos $LSE^{x}_{m,0}$

$$\frac{\sqrt{\mu_1\varepsilon_1}}{\mu_1}\cot\left(\omega_c\sqrt{\mu_1\varepsilon_1}\cdot\left(a-(w_2+w_1)\right)\right)=\frac{\sqrt{\mu_2\varepsilon_2}}{\mu_2}\cot\left(\omega_c\sqrt{\mu_2\varepsilon_2}\cdot(w_2)\right)$$

No guia carregado com 2 meios dielétricos obtém-se a freqüência de corte para os modos $LSM^{x}_{m,0}$

$$\frac{\varepsilon_1}{\sqrt{\mu_1\varepsilon_1}}\cot\left(\omega_c\sqrt{\mu_1\varepsilon_1}\cdot\left(a-(w_2+w_1)\right)\right)=\frac{\varepsilon_2}{\sqrt{\mu_2\varepsilon_2}}\cot\left(\omega_c\sqrt{\mu_2\varepsilon_2}\cdot(w_2)\right)$$

proximação 1 :

ara valores de $\omega_c = 2\pi\cdot f_c$, solução

umérica das equações transcendentais

om $w_2 \to \infty \Leftrightarrow a \to \infty$ e determinar W_1

Realidade : Ajustar W_1 , R, gap para a f_c desejada

Modos Transmitidos

$S_{21} \Leftrightarrow [T_{21}]$

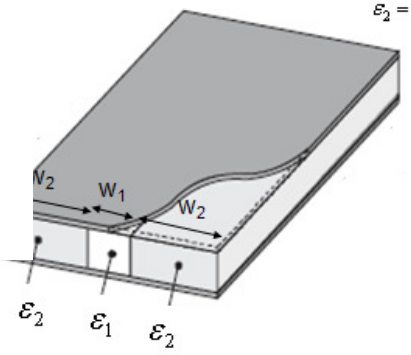
Solução não analítica = solução numérica

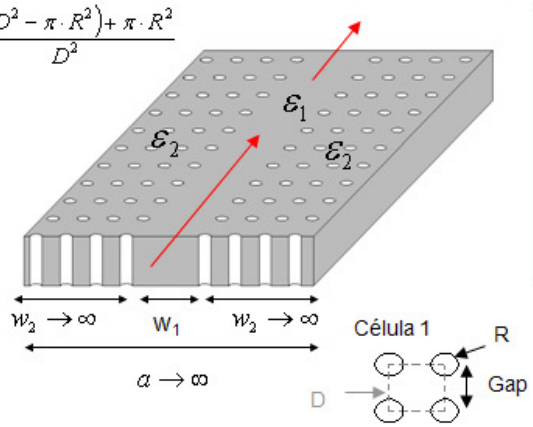
CST , HFSS

Meio 2 não homogêneo

Estrutura periódica

$$\varepsilon_2 = \frac{\varepsilon_1\cdot\left(D^2-\pi\cdot R^2\right)+\pi\cdot R^2}{D^2}$$

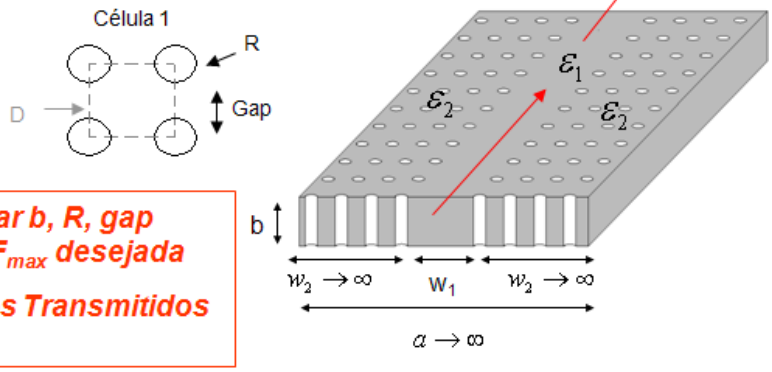




Dimensões do guia NRD :

$$\varepsilon_2 = \frac{\varepsilon_1 \cdot \left(D^2 - \pi \cdot R^2\right) + \pi \cdot R^2}{D^2}$$

$S_{21} \Leftrightarrow [T_{21}]$



No guia carregado com 2 meios dielétricos a freqüência de corte para os modos :

$$\frac{1}{2b\sqrt{\mu_2\varepsilon_2}} > f_c\left(LSE^{x}_{0,1}\right) > \frac{1}{2b\sqrt{\mu_1\varepsilon_1}}$$

$$\frac{1}{2b\sqrt{\mu_2\varepsilon_2}} > f_c\left(LSM^{x}_{0,1}\right) > \frac{1}{2b\sqrt{\mu_1\varepsilon_1}}$$

Ajustar b, R, gap para F_{max} desejada

Modos Transmitidos S_{21}

Sendo $\mu_2\varepsilon_2 < \mu_1\varepsilon_1$

imação 2 : $f_c = \frac{1}{2b\sqrt{\mu_2\varepsilon_2}} = \frac{1}{2b\sqrt{\mu_0\varepsilon_0\varepsilon_2}} = \frac{c_0}{2b\sqrt{\varepsilon_2}}$

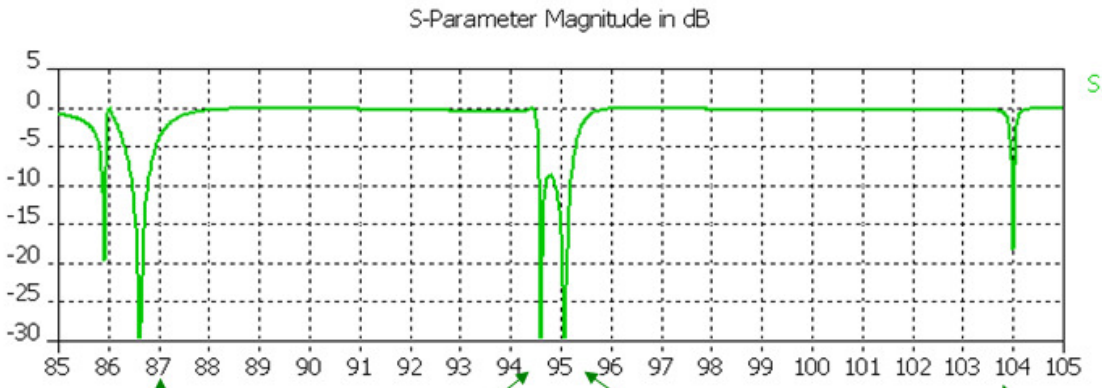
c = Fmax

uia transversal Guia longitudinal

$$\frac{c_0}{2 \cdot b \cdot \sqrt{\varepsilon_2}} = F_{Max}$$

Fmax Guia longitudinal				
	Substrato Er = 9,9 = E_1 Alumina		Substrato Er = 8,9 = E_1 Alumina	
	Gap (mm) 0,127	Gap (mm) 0,254	Gap (mm) 0,127	Gap (mm) 0,254
R vias (mm)	Fmax (GHz)	Fmax (GHz)	Fmax (GHz)	Fmax (GHz)
0,2	97,48	87,52	102,36	92,09
0,25	101,14	90,41	106,12	95,08
0,3	104,20	93,01	109,26	97,77
0,4	109,03	97,47	114,19	102,36
0,5	112,65	101,14	117,89	106,12
0,6	115,48	104,20	120,76	109,26
0,7	117,75	106,80	123,06	111,92
0,8	119,61	109,03	124,94	114,19

Exemplo de um guia NRD e sua simulação (CST)



$S_{21} \Leftrightarrow [T_{21}]$

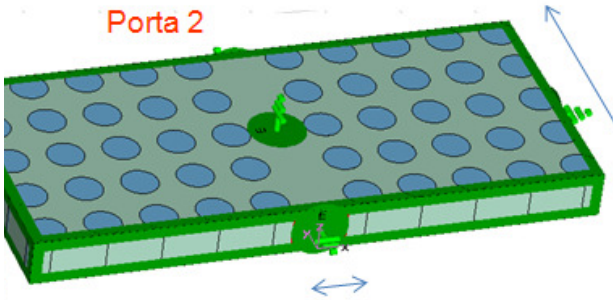
EBG
Electromagnetic
Band Gap

$f_{C_{(1^\circ\ Banda)}}(3dB) \approx 87GHz$

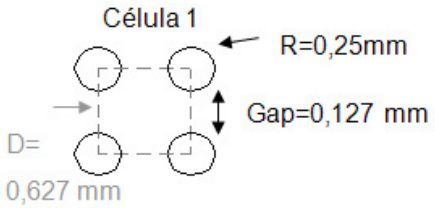
$F_{\max_{(1^\circ\ Banda)}}(3dB) \approx 94,7GHz$

$f_{C_{(2^\circ\ Banda)}}(3dB) \approx 95,5GHz$

$F_{\max\ (2^\circ\ Banda)}(3dB) \approx 103,8GHz$



$L \rightarrow \infty$



Alumina $\varepsilon_r = 9,9$

Anexo 5 - Publicação 1

http://www.esss.com.br/events/ansys2010/pdf/22_6_1230.pdf

2010 ANSYS SOUTH AMERICAN CONFERENCE & ESSS USERS MEETING
October 19-22 - Atibaia, SP - Brazil

FR-4 Substrate Integrated Waveguide PCB at 20GHz

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Centro de Estudos em Telecomunicações
Laboratório de Sistemas Ópticos, Microcircuitos e Microondas
GSOM - CETUC / PUC-Rio

Co-autores: ***Marbey Manhães Mosso*** – GSOM/ CETUC / PUC-Rio
Rodolfo Araujo de Azevedo Lima – IPqM / Marinha do Brasil

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Presentation Topics

- Problem Description: 1-Gb/s and 10-Gb/s PCB
- Methodology: Using HFSS 12 (Ansoft 3D Full-wave Electromagnetic Field Simulation) and Designer RF 5 (Product Suites for RF and microwave circuits design with embedded HFSS EM simulation)
- Comparison of experimental and simulated results
- Conclusion and next steps.

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oblem Description: 1-Gb/s and 10-Gb/s PCB

High Speed digital circuits are being implemented with serial/parallel processing;

- PCBs that use the commercial substrate (FR-4) in the above specified rates demand high complexity electronic processing to solve the planar lines issues: loss, crosstalk, delay etc.;
- Application of this work: to use Substrate Integrated Wave Guides (SIWG) to replace planar lines in the inter-chip communications on printed circuit boards.

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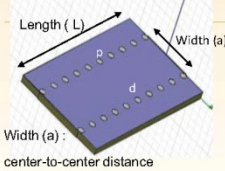
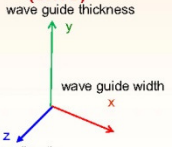
SIWG mapped to a RWG

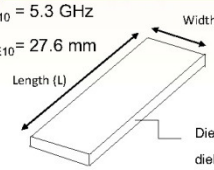


- Cooper metallization thickness (t=0.035mm) (top and bottom)
- Dielectric thickness (h =1.575mm)
- Dielectric constant (Εr = 4.3 FR-4) (inside)
- Wall of metalized via-holes with diameter (d=1.7 mm)
- Center-to-center spacing of via-holes in the wall (p = 4.6 mm)

Substrate Integrated Waveguide (SIWG)



f_{cTE10} = 5.3 GHz
λ_{fcTE10} = 27.6 mm



Cooper metallization thickness (t)

Dielectric thickness (h) with dielectric constant (Εr)

Rectangular Wave Guides (RWG)

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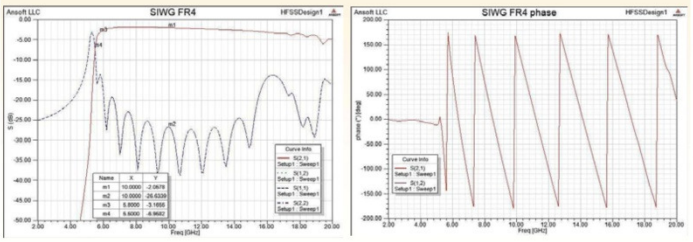
Simulated (HFSS) frequency response of the SIWG and equivalent phase



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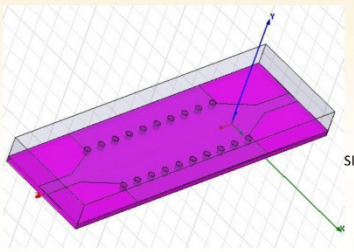
Prototype SIWG

Manufactured using LPKF PCB prototyping machine



Microstrip length to connector L_c = 20.00 mm

SIWG length L = 42.72 mm

Microstrip length to connector L_c = 20.00 mm

Microstrip length transition to waveguide L_{mg} = 9.10 mm

Microstrip width W_m = 3.24 mm

Includes:
- two SMA connectors;
- microstrip / waveguide transition in FR4 lossy substrate

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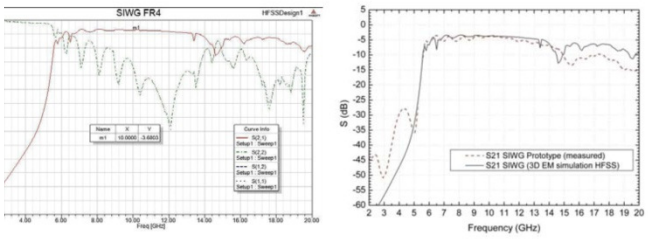
Comparison of experimental measurement of fabricated prototype and 3-D EM simulation (HFSS)

S – Parameters (dB)



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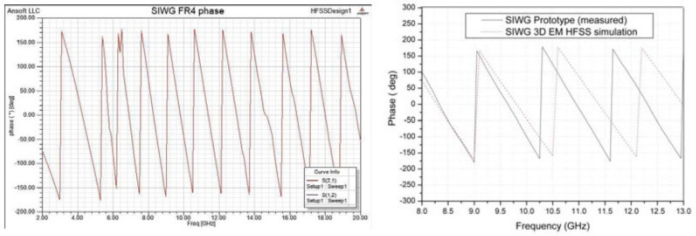
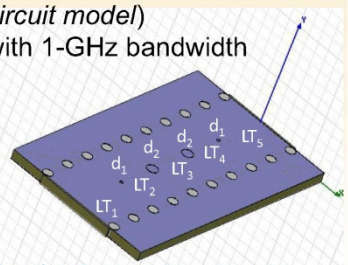
Comparison of experimental measurement of fabricated prototype and 3-D EM simulation (HFSS)

S – Parameters (Phase)

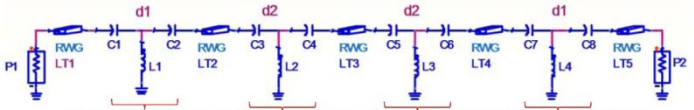


SIWG Filter – (*equivalent circuit model*)
10-GHz center frequency with 1-GHz bandwidth

- Waveguide length 1 and 5 – LT1 =LT5=10.00mm
- Waveguide length 2 and 4 – LT2=LT4=7.22 mm (Center-to-center distance between d1 and d2)
- Waveguide length 3 – LT3 = 8.28 mm (Center-to-center distance between d2 and d2)
- Waveguide thickness – b=1.575 mm
- Waveguide width - a= 13.80mm (Center –to-center distance wall)
- Via-hole diameters1 - d1= 0.50 mm
- Via-hole diameters 2 – d2=1.90mm
- Via –hole wall diameter d=1.7 mm
- Center – to center via hole wall p=4.6 mm



The model consists of five cascaded sections of the Rectangular Waveguide model



alternated with four equivalent PI circuits model for each centered metalized via-holes.

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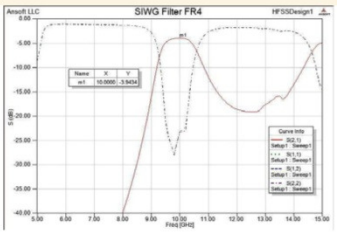
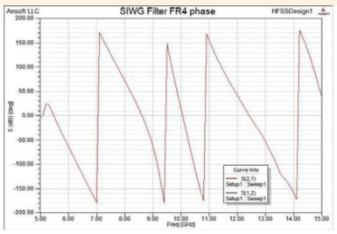
Frequency response of SIWG filter centered at 10 GHz with 1 GHz bandwidth





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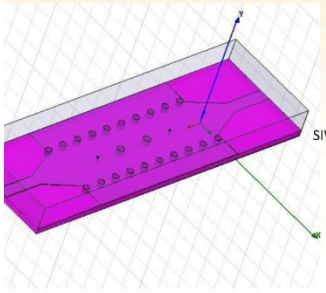
Prototype SIWG Filter



Microstrip length to connector L_c = 20.00 mm

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Microstrip length transition to waveguide L_{mg} = 9.10 mm

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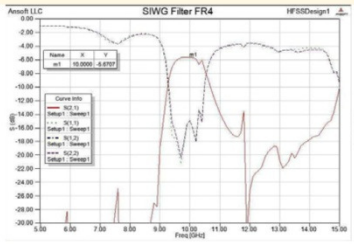
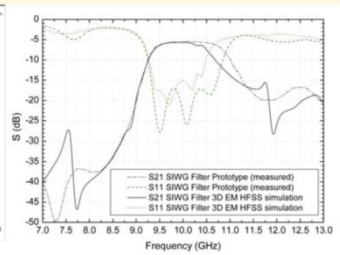
Comparison of experimental measurement of fabricated prototype Filter and 3-D EM simulation (HFSS)

Frequency response of SIWG filter centered at 10 GHz with 1 GHz bandwidth





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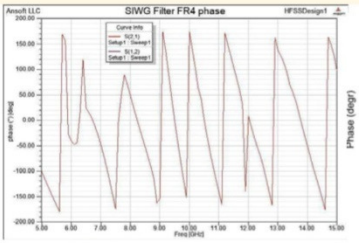
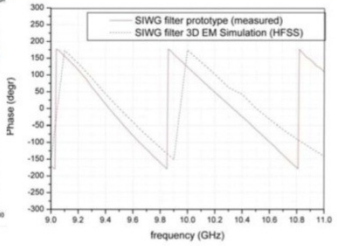
Comparison of experimental measurement of fabricated prototype Filter and 3-D EM simulation (HFSS)

Phase of SIWG filter in the bandwidth





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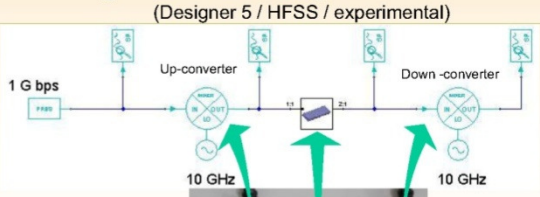
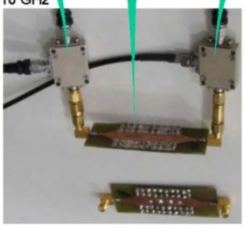
1-Gb/s digital circuit using SIWG FR-4 substrate

(Designer 5 / HFSS / experimental)





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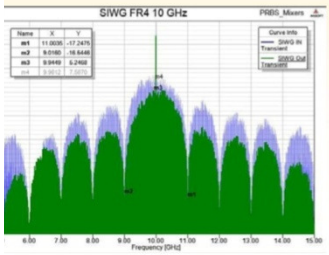
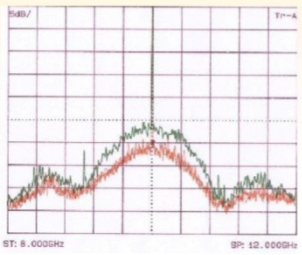
Waveguide: experimental measurement vs. simulation

nparison of experimental measurement and Simulated Spectrum ponse for 1 Gb/s NRZ formats





pagated PRBs signal = up converter (10 GHz)

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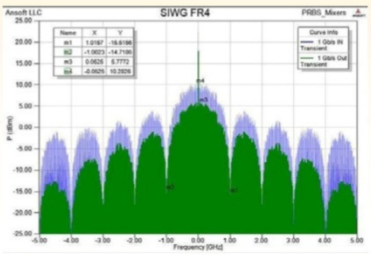
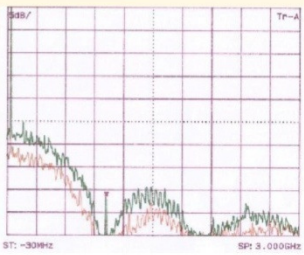
Waveguide: experimental measurement vs. simulation

Comparison of experimental measurement and Simulated Spectrum response for 1 Gb/s NRZ formats





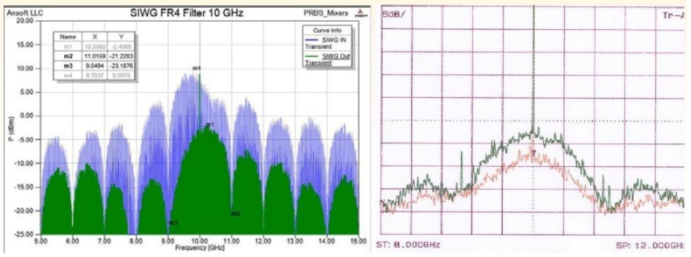
Received PRBs signal = down converter

ANSYS ESSS

2010 ANSYS SOUTH AMERICAN CONFERENCE & ESSS USERS MEETING

Filter:
experimental measurement vs. simulation

Comparison of experimental measurement and Simulated Spectrum response for 1 Gb/s NRZ formats



Propagated PRBs signal = up converter

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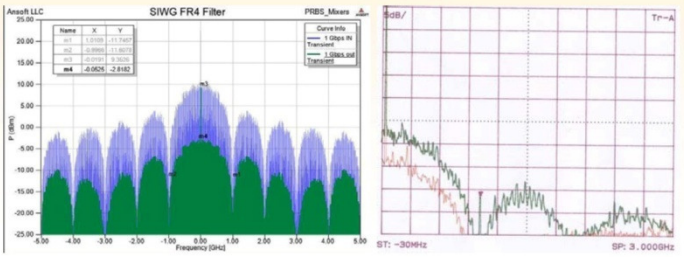
Filter:
experimental measurement vs. simulation

Comparison of experimental measurement and Simulated Spectrum response for 1 Gb/s NRZ formats

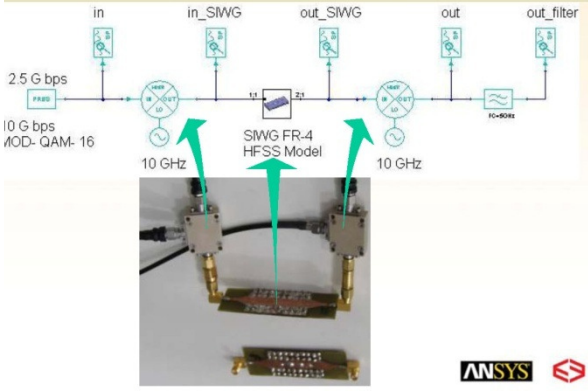


Received PRBs signal = down converter

2010 ANSYS SOUTH AMERICAN CONFERENCE & ESSS USERS MEETING

10-Gb/s digital circuit using SIWG FR-4 substrate

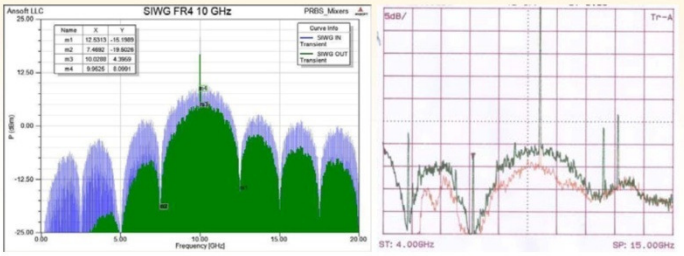
(Designer 5 / HFSS / experimental)



2010 ANSYS SOUTH AMERICAN CONFERENCE & ESSS USERS MEETING

Waveguide:
experimental measurement vs. simulation

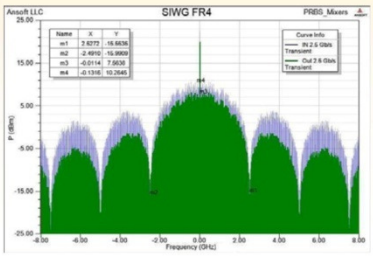
Comparison of experimental measurement and Simulated Spectrum response for 10 Gb/s 16-QAM modulated NRZ formats

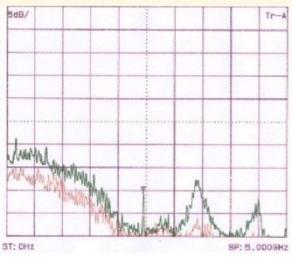


Propagated PRBs signal = up converter (10 GHz)

Waveguide: experimental measurement vs. simulation

Comparison of experimental measurement and Simulated Spectrum response for 10 Gb/s 16-QAM modulated NRZ formats

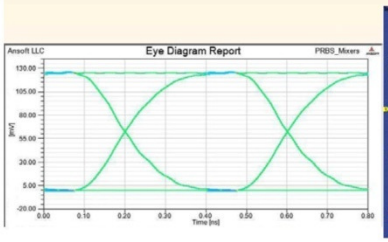




Received PRBs signal = down converter

Waveguide: experimental measurement vs. simulation

Comparison of experimental measurement and Simulated Eye Diagram / BER in 10 Gb/s 16-QAM modulated NRZ formats



Received PRBs signal = down converter

Conclusion and next steps

Using HFSS 12 (Ansoft 3D Full-wave Electromagnetic Field Simulation) and Designer RF 5 (Product Suites for RF and microwave circuits design with embedded HFSS EM simulation) a waveguide and a filter were modeled and simulated using a commercial FR-4 lossy dielectric substrate, based on the concept of Substrate Integrated Wave Guides (SIWG) to replace the planar lines in inter-chip 1Gb/s and 10Gb/s digital circuits. A set of measured experimental results was evaluated, showing excellent agreement with simulation predictions and far than satisfactory performance.

The excellent results achieved indicate that several components operating up to 10 GHz (and maybe 20 GHz) could be realized with the commercial FR-4 substrate in the PCB inter-chip connections, employed in this work.

Besides this work, new applications in telecommunications ultra-fast electronics circuits involving BPSK, 16QAM and 64QAM modulation formats associated with 10 Gb/s and 100 Gb/s waveguide propagation are being achieved in the our research center.

Acknowledgment

This work was partially supported by Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), Brazil.

The author is grateful to MOLOGNI, Juliano Fujioka (ESSS - Engineering Simulation & Scientific Software) for computational assistance.

Anexo 6 - Publicação 2

Substrate Integrated Wave Guide Filter at 10 GHz Using Commercial FR-4 Lossy Substrate

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Abstract—***Based on the concept of Substrate Integrated Wave Guides (SIWG), a filter centered in 10GHz with 1-GHz bandwidth is modeled, simulated and fabricated using a commercial FR-4 lossy dielectric substrate. A low-cost printed circuit board manufacturing technique is employed. A set of experimental results obtained is evaluated, showing excellent agreement with simulation predictions and far than satisfactory performance.***

Keywords–SIWG; waveguide; microwave filter; FR-4; printed circuit board.

I. INTRODUCTION

Recently, the concept of the Substrate Integrated Wave Guide (SIWG) component has been proposed [1],[2] for wireless interconnects at millimeter-wave frequencies [3],[4],[5] and at ultrahigh-speed digital applications able to operate at data rates up to 50 Gbit/s, 100 Gbit/s or 200 Gbit/s [6], [7]. These components also can be applied in military radar systems with frequency agility.

SIWGs can be realized with a linear array of metalized via-holes or metal posts embedded in the same substrate used for the planar circuit [1],[2]. Several transition structures have been proposed [8] to excite the dielectric guide. In all these structures, the rectangular wave guide and the planar circuits (such as microstrip line or coplanar waveguide) are built onto the same substrate and the transition is formed with a simple EM matching geometry between both structures [9], [10].

In this work, a lossy commercial dielectric substrate was selected in which SIWG microwave components are developed. In order to demonstrate the potentials of the FR-4 dielectric substrate using a low-cost printed circuit board fabrication technique, a substrate wave guide filter centered in 10 GHz was designed, simulated, fabricated and characterized experimentally.

This paper is organized as follows. After the present introduction, Section II presents the theoretical model for the waveguide and the filter, and also the simulations carried out at Agilent™ Advanced Design System (ADS) [11] and CST Microwave Studio® [12] software platforms. In Section III, the fabrication of the waveguide and the filter are described, along with the experimental results obtained. Also in section III, a comparative analysis between the results and simulations is performed. In section IV, some comments and conclusions are presented.

II. SIWG AND FILTER DESIGN

The Substrate Integrated Waveguide configuration consists of a dielectric substrate whose boundaries in both sides are walls consisted of parallel arrays of metalized via-holes [1]. This structure can be related to an dielectric rectangular waveguide (RWG) [1], [2].

Fig. 1 illustrates (a) a three-dimensional view of a SIWG and (b) its rectangular waveguide equivalent model. The SIWG was designed using a FR-4 substrate with the following characteristics: loss tangent $tan\delta = 0.019$, dielectric constant $\varepsilon_r = 4.3$, thickness $h = 1.575$, and cooper metallization thickness $t = 0.035$mm. In Fig. 1(a), d is the via-hole diameter and p is the center-to-center spacing of the via-holes in the matrix wall.

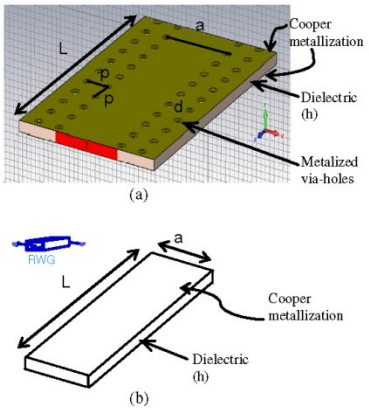

Figure 1. Substrade integrated wave guide mapped to a rectangular waveguide: (a) 3D view of SIWG [12] and; (b) equivalent rectangular waveguide representation.

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Aiming at obtaining minimum radiation loss and best return loss characteristics,[2],[3],[10], the parameters of the via-hole array, i.e. hole diameter d and spacing p, are optimized by electromagnetic frequency domain simulation using CST Microwave Studio three-dimensional electromagnetic application. A cut-off frequency of 5.3 GHz was considered, with TE_{10} mode excitation and SIWG width a = 13.8 mm, and the values d = 1.7 mm and p = 4.6 mm were obtained.

A dielectric rectangular waveguide with the same cut-off frequency, same width and thickness, according to the relation in Fig. 1(b), is also evaluated, using ADS S-parameter circuit simulation. In both cases, a reference impedance Z_c= 50 Ω is considered for the design, and the length used in the simulations was L = 42.72 mm.

Fig. 2 shows the electromagnetic simulated reflection loss (S_{11}) and transmission loss (S_{21}) for the SIWG together with S-parameter simulations for the rectangular dielectric wave guide. In both cases, the insertion loss within the waveguide bandwidth at 10 GHz is approximately 2 dB. It can be observed that the simulated SIWG and the dielectric RWG present very similar results.

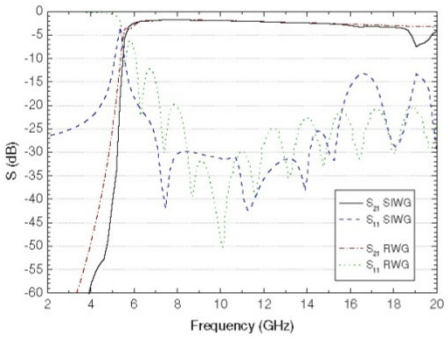

Figure 2. Simulated frequency response of the SIWG and the equivalent RWG.

Considering the simulated results obtained for the waveguides, a new method is proposed aiming at the design of a waveguide filter. The filter configuration adopted consists of the insertion of centered via-holes located inside the SIWG [10]. The via-holes can be alternatively regarded as centered inductive metal posts in a rectangular wave guide [13], [14], [15].

Fig. 3(a) illustrates the three-dimensional schematic view of the SIWG multi-pole filter configuration, using two pairs of posts, symmetrically disposed in relation to the longitudinal center of the filter. In Fig. 3, the physical dimensions are represented: a and b are, respectively, the waveguide width and height, d is the post diameter and LT is the distance between post elements. Fig. 3(b) depicts the cross section of the waveguide with a centered via-hole. Fig 3(c) shows the PI equivalent circuit model for each metalized centered via-hole [15].

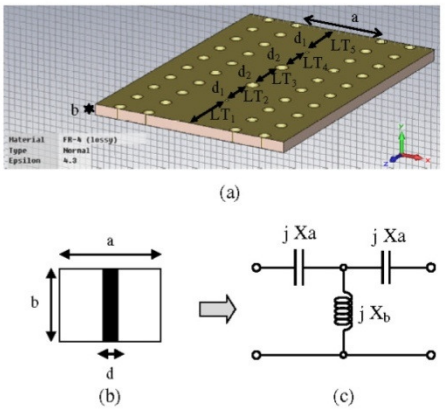

Figure 3. SIWG filter configuration with centered via-hole: (a) three-dimensional schematic view [12] ; (b) cross-section of via-hole and its physical parameters and; (c) mapping of via-hole as a PI network model.

In the PI equivalent circuit, the relations between the dimensions a and b of the rectangular guide, the centered via-hole diameters d, the inductive reactance (Xb), the capacitive reactance (Xa), the wavelength and wave impedance of the waveguide propagating mode (TE_{10}) in the RWG, were presented by Marcuvitz' theory and can be found in [15].

According to the equivalency relations presented in Figs. 1 and 3, a possible filter equivalent circuit is proposed, as illustrated in Fig. 4. The model consists of five cascaded sections of dielectric rectangular waveguides alternated with four PI networks, corresponding to the four centered posts. These elements are calculated, using the previously mentioned relations, for filter center frequency at 10 GHz and 1-GHz bandwidth. This calculation is a good initial approximation, and the values found are fed to the ADS circuit model, as depicted in Fig. 4. Using the software optimization procedures, these parameters are adjusted to yield better filter performance. The values obtained were then a = 13.8 mm, b = 1.575 mm, $d1$ = 0.5 mm, $d2$ = 1.9 mm, $LT1_{length}$ = 10 mm, $LT2_{length}$ = 7.22 mm, $LT3_{length}$ = 8.28 mm, $LT4_{length}$ = 7.22 mm and $LT5_{length}$ = 10 mm obtain a SIWG filter with 42.72 mm length.

Figure 4. Circuit model for a SIWG filter with centered via-hole [11] .

Afterwards, electromagnetic simulations were carried out at CST Microwave Studio for the SIGW filter using the dimensions obtained from the model optimization, according to the configuration in Fig. 3(a). The simulated S-parameters are presented in Fig. 5: reflection loss (S_{11}) and transmission loss (S_{21}). The equivalent circuit filter design using ADS S-parameter simulations is also represented for comparison, showing good agreement.

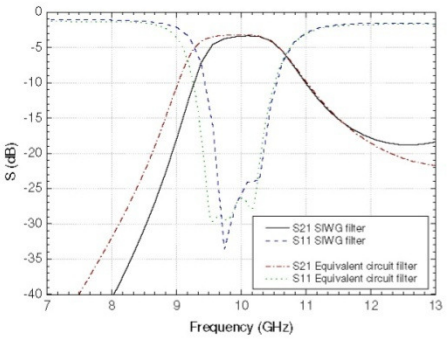

Figure 5. Frequency response of SIWG filter eletromagnetic frequency domain simulation and RWG equivalent circuit filter design with S parameters simulation.

It is important to verify that the simulation of the circuit model and the electromagnetic simulated SIWG filter present compatible results. Small discrepancies are observed since the circuit model is an auxiliary design approximation, closely verified by the posterior, and more accurate, EM simulation. The insertion loss in the center frequency in both cases is approximately 3.3 dB.

The procedures adopted, combining the posts analytical PI models, SIWG-RWG equivalency, circuit simulations and optimization, avoid extensive analytical methods and represent a significant simplification in the design solution.

III. Experimental Results

Using a LPKF™ Printed Circuit Board prototyping machine, a SIGW waveguide and the filter were fabricated on a FR-4 substrate. The access to both the waveguide and the filter was performed by microstrip lines, using a simple matching geometry between the guide and the connector as a microstrip linear width transition [9], [16]. A photograph of the prototype of the waveguide is shown in Fig. 6(a). The fabricated filter is portrayed in Fig. 6(b).

All via-holes and post holes where perforated by the prototype machine drills. The metallization was accomplished with metal vias soldered manually, respecting the adequate diameters. The access to the circuit was made through 3.5 mm coaxial (SMA) connectors and 50-Ω 3.24 mm wide microstrip lines. The microstrip width transition was 9.1-mm long.

The frequency response of the prototype SIWG was measured using an Agilent HP 8720C Vector Network Analyzer. Fig. 7 presents the comparison of EM simulation and measured results for the SIWG waveguide. It can be noticed from the figure that the cut-off frequency is the same in the both cases.

The insertion loss in 10 GHz for the simulated waveguide is approximately 2 dB and for the measured guide is 4 dB. This difference between measurement and simulation occurs because the prototype includes two cross-sectional structure transitions (i.e. the SIWG to microstrip transition at both ends) not evaluated in the simulated components. This and the additional loss along 40 mm of microstrip lines are responsible for the small 2.5 dB insertion loss difference found.

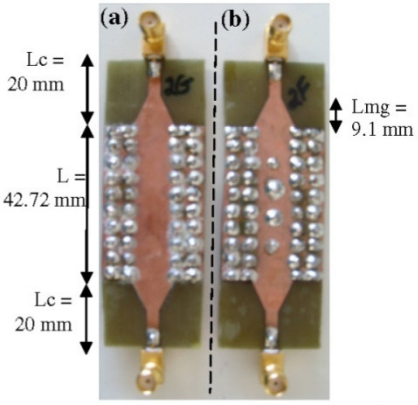

Figure 6. Fabricated prototypes: (a) SIWG; (b) SIWG filter.

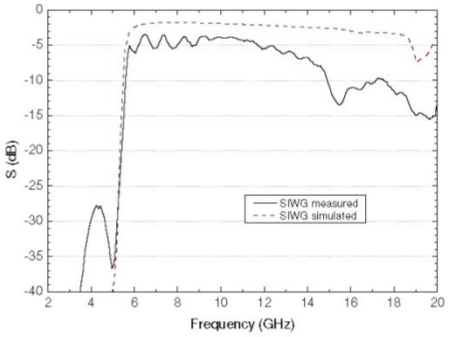

Figure 7. Frequency response of SIWG: comparison of experimental measurement of fabricated prototype and EM simulation.

Then, the frequency response of the SIGW filter was also characterized experimentally. Fig. 8 presents the comparison of reflection loss (S_{11}) and transmission loss (S_{21}) obtained by EM simulation and the measured results for the filter prototype. The measured filter showed an insertion loss of approximately 5.8 dB while the predicted insertion loss from the simulation was 3.34 dB. This difference between the measured and the simulated model is attributed to the same reasons discussed above for the SIWG.

Fig. 9 presents the experimental measurement of the phase characteristics of the SIWG prototype filter within the bandwidth and its vicinity. It was verified that the phase variation is linear with frequency, a quite desirable feature. The same Fig. 9 also presents the measured results in the same

frequency range for the group delay of the system. It can be observed that delay is mostly constant over the filter bandwidth.

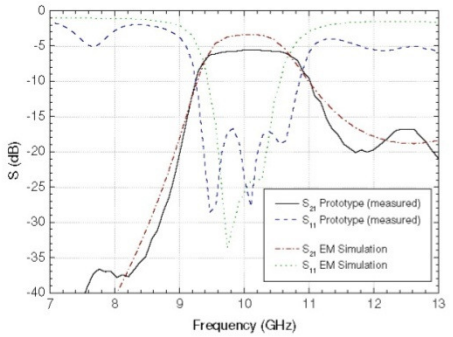

Figure 8. Frequency response of the SIWG 10-GHz filter: comparison of experimental measurement of fabricated prototype and EM simulation.

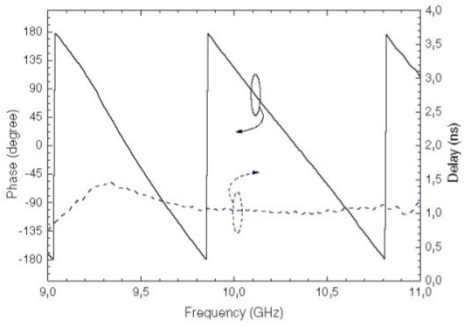

Figure 9. Measured phase characteristics and group delay of the SIWG filter fabricated prototype.

IV. Comments and Conclusions

Low loss dielectric substrates are being used to realize components up to 200 GHz. In this paper, a lossy substrate (FR-4) is used to achieve a 10-GHz central frequency with 1-GHz band filter.

A simplified procedure, associating the electromagnetic response of a SIWG multi-pole filter with its respective filter model represented by S-parameter simulations is presented and corresponds to a new approach to the design procedure in this field. Excellent agreement was observed between the results from S-parameter model simulation and electromagnetic simulation carried out, for both the SIWG waveguide and filter. The transitions between 50-Ω coaxial lines and the prototyped waveguide filter stood for approximately 2 dB in the insertion loss.

Both the substrate integrated waveguide and the SIWG filter were fabricated using very simple fabrication techniques. The measured experimental results obtained demonstrate that the simplified process adopted is helpful in the design of components through waveguide configurations. Moreover, the excellent experimental results achieved indicate that several components operating up to 10 GHz (and maybe 20 GHz) could be realized with the commercial FR-4 substrate employed in this work.

Applications in Telecommunications, ultra-fast electronics circuits and military tracking radars could be achieved with significant simplification and cost reduction.

Acknowledgment

This work was supported by Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), Brazil.

The authors acknowledge the use of FDTD software CST Microwave Studio® under the CST Co-operation License Agreement with CETUC/PUC-Rio. The authors also acknowledge the use of the Advanced Design System (ADS) electronic design software platform through Agilent EEsof EDA university educational support program for CETUC/PUC-Rio. The author is grateful to Nascimento F. A. S. and Novo, M. S. for computational assistance.

The circuits were fabricated and assembled at the Microwave and Optical Systems Lab with cooperation of the Optoelectronics and Instrumentation Lab, both at CETUC/PUC-Rio, Brazil. All microwave measurements were carried out at CETUC microwave lab.

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Anexo 7 - Publicação 3

FR-4 Waveguide Electronic Circuits at 10 Gbit/s

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Abstract—**A 10-Gbit/s interconnection using a FR-4 Substrate Integrated Waveguide (SIWG) and ASK and QAM modulation format is evaluated as a new alternative for high-speed digital electronic circuits. A set of experimental and simulation results obtained is evaluated, showing far than satisfactory performance.**

Keywords-SIWG (substrate integrated waveguide); FR-4 printed circuits boards (PCB); high-speed digital electronic circuits, Gigabit Ethernet

I. INTRODUCTION

Stream parallelism is usually employed in interchip ultra fast digital electronic circuits, as in the 10GbE standard [1], in order to overcome the speed limitations of the lines. However, the parallel microstrip lines still carry high speed digital signals, which can be subject to undesired effects such as crosstalk and skin effect. Substrate Integrated Waveguide (SIWG) configurations present lower insertion loss, better noise characteristics and higher cross-talk immunity when compared to microstrip and other planar lines [2, 3].

Recently, a substrate integrated waveguide using commercial FR-4 lossy substrate has been proposed, fabricated (using very simple fabrication techniques) and tested by the authors [4]. The measured experimental results obtained demonstrated that the simplified process adopted is helpful in the design of printed circuit boards (PCB) up to 20 GHz that could be realized using FR-4 SIWG configurations.

The SIWG waveguide highpass behavior related to the cut-off frequency of the first propagating mode jeopardizes signal integrity of digital NRZ/RZ streams, since it fades the digital stream's DC component and low frequency characteristics [5]. To overcome this limitation, this work proposes a serial digital interconnection using modulation formats integrated with the FR-4 waveguide for up to 10 Gbit/s rates.

The remainder of this paper is organized as follows. Section II introduces the gigabit properties of a prototype FR-4 SIWG. In Section III, experimental transmission of a 2.5-Gbit/s sequence through the SIWG is carried out. Section IV assesses the transmission of QAM formats in the SIWG, which is evaluated by the simulation of a 16-QAM setup. Finally, section V presents some comments and conclusions of this work.

II. FR-4 SIWG DIGITAL INTERCONNECTIONS

The FR-4 substrate integrated waveguide prototype, showed in Fig. 1, was designed and manufactured in the author's facilities at CETUC [4] using a LPKF Printed Circuit Board prototyping machine and microstrip-SMA connector transitions. The prototype was modeled using Ansoft's HFSS [7] three-dimensional full-wave electromagnetic field software, and simulated using its frequency-domain solver. The 3D model used for simulation is also depicted in Fig. 1.

The SIWG prototype was tested up to 20 GHz, and the experimental insertion and reflection losses, measured using an Agilent HP 8720C Vector Network Analyzer, are presented in Fig. 2. The simulated frequency response characteristics are also presented in Fig. 2 for comparison, showing excellent agreement.

In order to overcome the SIWG low-frequency constraint to serial digital interconnection, a modulation format can be applied to the signal, which is then shifted to, for example, a 10 GHz carrier frequency, so that all signal information is within the SIWG passband. In this work, both ASK and QAM are assessed.

Particularly, it is known that for digital QAM transmission, phase linearity is a key feature for signal integrity. The phase characteristics of the prototype was then investigated above the cutoff frequency and presented in Fig. 3, where measured and simulation results can be compared.

This work was partially supported by Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), Brazil.

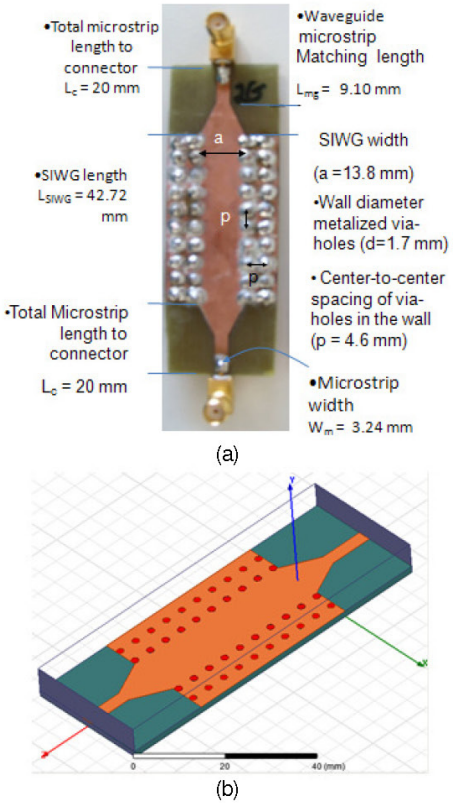

Figure 1. FR-4 Substrate Integrated Waveguide: (a) prototype; (b) 3D model on HFSS.

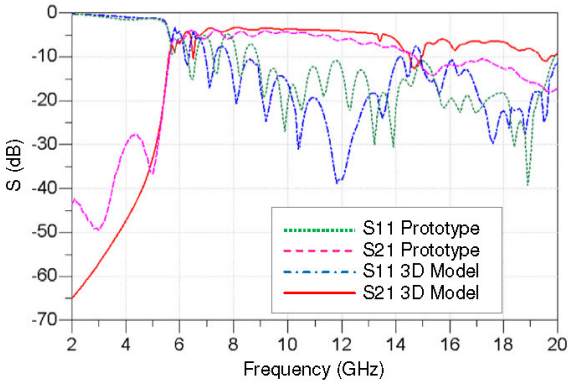

Figure 2. Insertion and return loss of a FR-4 SIWG prototype: comparison of experimental measurement and 3D EM simulation.

The results in Fig. 3 show very good agreement, and both exhibit a smooth linear phase response within the SIWG bandwidth around 10 GHz, indicating that the structure used in the prototype is suitable for the transmission of digital QAM signals.

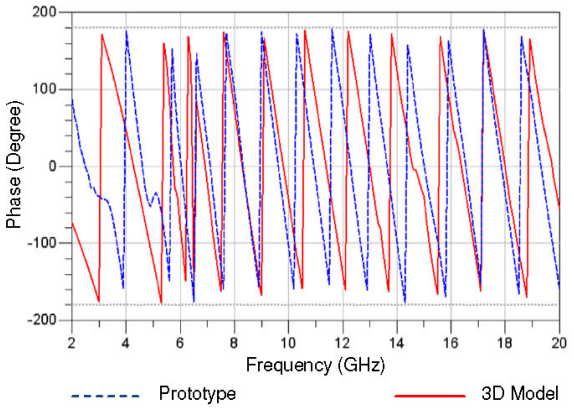

Figure 3. Phase characteristics of the FR-4 SIWG prototype: comparison of experimental measurement and 3D EM simulation.

III. TRANSMISSION WITH ASK MODULATION

An experimental setup was implemented for the test of a 2.5 Gbit/s sequence transmission through the prototype SIWG using ASK modulation at 10 GHz. A pulse generator (HP 8133) was used to generate the 2.5-Gbit/s PRBS. Two double balanced mixers placed in the ends of the SIWG were used as up and down converters, respectively shifting the signal up to the carrier frequency before the SIWG and back down to baseband after transmission through the SIWG. The 10-GHz carrier frequency was generated by a local oscillator and delivered to both mixers. Fig. 4 presents a photograph of the SIWG and mixers in the experimental setup.

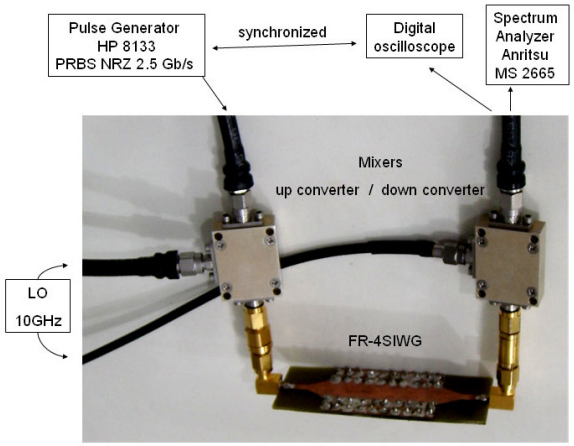

Figure 4. Experimental setup for the test of the transmission of a 10-GHz carrier modulated with a 2.5 Gbit/s PRBS through the FR-4 waveguide.

A spectrum analyzer (Anritsu MS 2665) was used to measure the signal spectrum in both ends of the waveguide and thus evaluate the signal transmission effects. Fig. 5 shows the great similarity between the signal spectrum measured at both the FR-4 waveguide input and output ends.

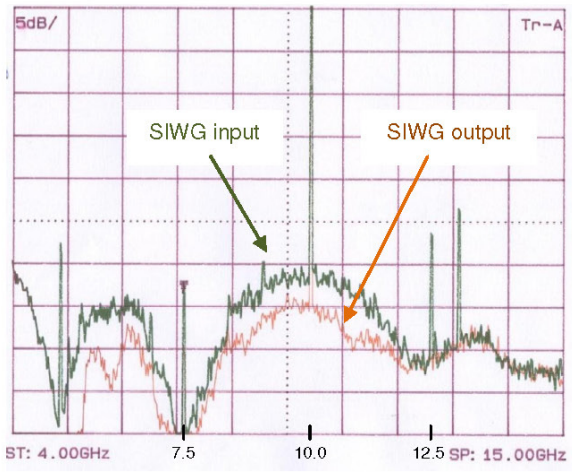

Figure 5. Digital Spectrum measured before and after the FR-4 SIWG.

The insertion loss of the waveguide does not greatly affect the digital signal performance – this can be seen by measuring the eye diagram with a digital oscilloscope at the down converter output port, synchronized with the PRBS source at 2.5 Gbit/s. Fig. 6 presents the measured eye diagram.

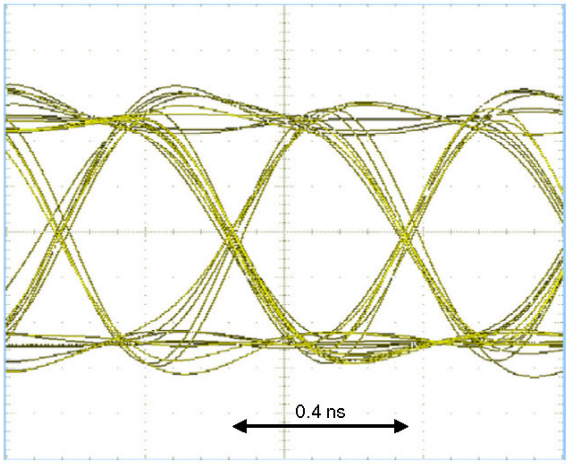

Figure 6. Eye diagram measured at the down converter output port, synchronized with the digital source at 2.5 Gbit/s.

IV. TRANSMISSION WITH 16-QAM MODULATION

When a 10 Gbit/s stream is modulated using a 16-QAM or 64-QAM format, the modulated signal has a 2.5 Gsymbol/s or 1.67 Gsymbol/s rate, respectively. These formats can be transported in the FR4 SIWG within the 5 GHz to 20 GHz bandwidth. Particularly, for a 16-QAM format, most of the signal energy will be concentrated between 7 and 13 GHz. Considering the greater bandwidth reduction using 64-QAM, a lower BER could probably be achieved. However, modulation and demodulation would become too complex [6, 9, 10] for this application.

Using 16-QAM format, the energy of the 10 Gbit/s signal will be concentrated in the same frequency passband as the ASK transmission of Section III. Nevertheless, QAM phase requirements on the transmission media are far more restrictive than those of an ASK signal. In spite of that, it has been seen from Fig. 3 that the prototype SIWG exhibits a fairly linear phase response in the desired frequency passband, indicating that it is appropriate for QAM transmission.

Therefore, a 10 Gbit/s bit stream can be modulated in 16-QAM format and transported by a FR-4 SIWG as is proposed in the block diagram of Fig. 7. In the destination end, 16-QAM demodulation is employed. The TX and RX oscillators must be synchronized and a 10 GHz carrier is obtained.

Fig. 8 presents a Modulation/Demodulation 16-QAM digital circuit model using Product Suites for RF and microwave circuits design with embedded HFSS EM simulation [7, 8]. This is the QAM simulation topology proposed by Ansoft Circuit Designer documentation.

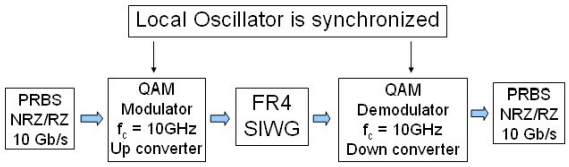

Figure 7. FR-4 substrate integrated waveguide 10-Gbit/s Serial QAM digital interconnection block diagram.

In the model of Fig. 8, a digital 10-Gbit/s PRBS sequence is generated. A QAM block yields in-phase and quadrature sequences for the 16-QAM digital signal, which are re-sampled in order to adapt the sampling rate for the digital signal simulation of the QAM signal. A digital filter eliminates spurious and both signals are then amplified and used to generate the digital 16-QAM signal at 10 GHz in the IQMOD block. The parameters for the digital filter, digital amplifier and sampler were chosen for a 16-QAM format in 10Gbit/s rate [6, 9, 10], considering a 10-GHz carrier.

In Fig. 8, the signal spectrum is evaluated before and after the SIWG. The simulated spectrum of the 16-QAM 10 Gbit/s sequence using the proposed modulation scheme is presented in Fig. 9, in hatched blue. This sequence was propagated through the model of the FR-4 SIWG prototype and the output spectrum of the QAM signal is also depicted in Fig. 9, in solid green.

Then, the propagated signal is demodulated, using the demodulation scheme proposed in Fig. 8. In order to evaluate the degradation of the signal, Fig. 10 depicts the comparison of simulated eye diagrams for both transmitted and received signals. The differences are almost imperceptible to a visual analysis. The average BER (bit error rate) was estimated, resulting approximately 10^{-8}.

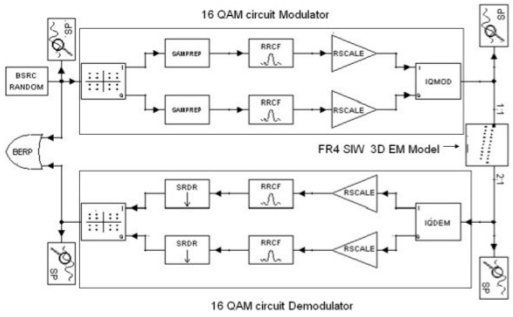

Figure 8. Circuit schematics for simulation of 16-QAM modulation/ demodulation integrated with a FR-4 waveguide in 3D EM model [7, 8].

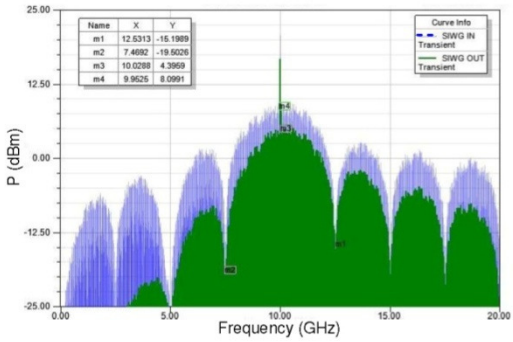

Figure 9. Simulated signal spectrum of 10-Gbit/s 16-QAM signal: SIWG IN before the waveguide, in hatched blue; and SIWG OUT after propagation through the waveguide, in solid green.

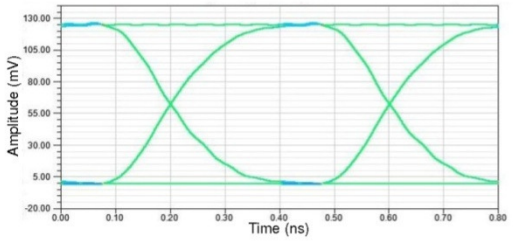

Figure 10. Simulated signal eye diagram of 10-Gbit/s 16-QAM signal: before, in blue, and after propagation through the waveguide, in green.

V. COMMENTS AND CONCLUSION

The set of measured experimental results of a FR-4 SIWG prototype was evaluated, showing excellent agreement with simulation predictions and far than satisfactory performance. Experimental transmission of a 2.5-Gbit/s ASK signal at 10 GHz was performed. The results obtained indicated that the prototype SIWG was appropriate for QAM. Simulation of the transmission of a 10-Gbit/s 16-QAM signal at 10 GHz was carried out, showing good performance.

PCBs using the commercial lossy substrate FR-4 in the 10 Gbit/s rates demand high complexity electronic processing to solve the planar line issues, like loss, crosstalk, differential delay etc. According to the results in this work, FR-4 substrate integrated wave guides (SIWG) can be used to replace planar line parallel buses in the inter-chip communications on printed circuit boards at 10 Gbit/s, using serial digital interconnections instead of complex parallelism in electronic circuits.

In addition to this work, a set of activities in telecommunications ultra-fast electronics circuits involving BPSK, 16-QAM and 64-QAM modulation formats associated with 10 Gbit/s and 100 Gbit/s SIWG propagation are being carry out in our research center.

With the excellent simulated and experimental results for the FR-4 substrate integrated waveguide, a 10 GbEthernet standard can be proposed using a serial interchip connection on the PCB as cost reduction, better performance and simplicity using QAM modulation and demodulation format.

ACKNOWLEDGMENT

This work was partially supported by Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), Brazil.

The authors acknowledge the use of the Ansoft 3D Full-Wave Electromagnetic Field Simulation software platform support for CETUC/PUC-Rio

The circuits were fabricated and assembled at the Microwave and Optical Systems Lab with cooperation of the Optoelectronics and Instrumentation Lab, both at CETUC/PUC-Rio, Brazil. All microwave measurements and simulations were carried out at CETUC microwave lab.

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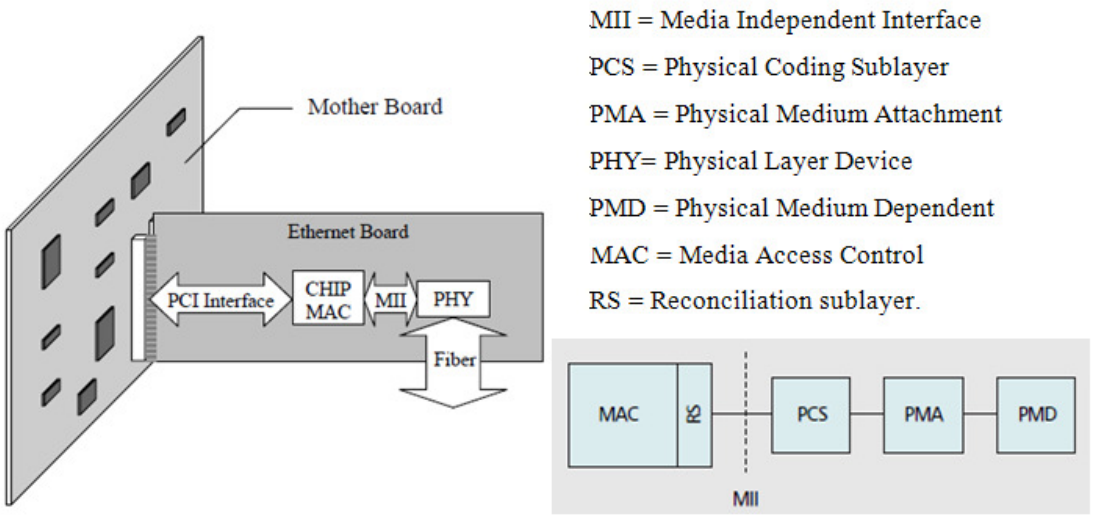
Anexo 8 : GB Ethernet

O Grupo de estudo de alta velocidade do IEEE (HSSG - Higher Speed Study Group) foi criado em resposta a uma chamada de Interesse (TPI - Call for Interest) para soluções de Ethernet de de altíssimas taxas de transmissão realizada durante a reunião plenária IEEE 802 em julho de 2006. O HSSG identificou os principais objetivos da Ethernet de alta velocidade e resultou na formação do P802.3ba IEEE Task Force (TF) [29] , em Dezembro de 2007. Desde então, o TF tem trabalhado nas especificações de projecto Ethernet 100Gb/s e 40Gb/s e em Novembro de 2009, lançou o projecto 3.0 [30], para ser aprovado, em Junho de 2010. No início o único alvo era a taxa de dados de 100 Gb/s Ethernet , mas depois considerando as aplicações de servidores e armazenamento, acrescentou-se as soluções de taxa de dados de 40 Gb/s. Atualmente, as duas taxas de dados são especificadas simultaneamente no padrão. A figura 12 apresenta em (a) a configuração do perfil de camadas padrão Ethernet e em (b) um exemplo de uma placa Ethernet. As Sessões seguintes deste capítulo abordarão as especificações e as características de cada taxa de bits envolvida.



Padrão do protocolo IEEE 802.3

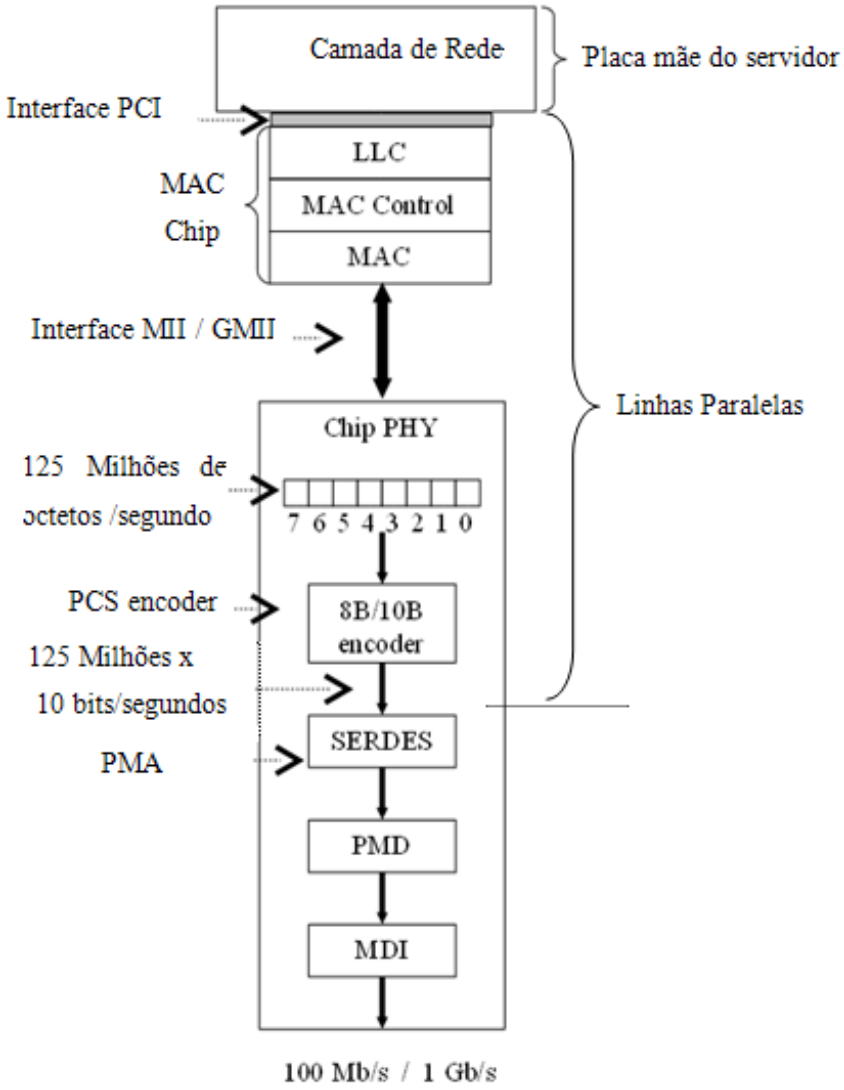
Ethernet 1Gb/s

A figura 23 representa o perfil das camadas MAC (Media Access Control) e PHY (física) de uma interface de rede operando nas taxas de 10MBs, 100MBs (Fast Ethernet) e 1Gbs, a partir da interface PCI (Peripheral Component Interface) localizada entre a placa mãe e o "chip" MAC. Na camada "MAC control", os endereços "MAC" origem e "MAC" destino são introduzidos no pacote de acordo com rigidos padrões do IEEE.

A camada física coleta informações da camada MAC através da interface GMII em aplicações Gigabit Ethernet (MII em Fast Ethernet). Funcionalidades da camada física podem ser implementadas através de "chip" PHY. Esses chips são capazes de executar mais de 150 milhões de operações de DSP (Digital Signal Processing) para lidar com a atenuação considerável, "crosstalk" e ecos que penalizam os sinais de alta velocidade. A primeira sub-camada, o PCS (Physical Code Sub Layer) implementa a auto-negociação para configurar automaticamente o link no modo full-duplex, nas taxas de 10Mb/s, 100Mb/s e 1Gb/s logo que a conexão é ativada. Outra tarefa importante nessa camada é a codificação e decodificação 8B/10B, recebendo 08 bits em paralelo a cada ciclo de "clock" das interfaces MII (MEDIA INDEPENDENT INTERFACE) / GMII (GIGABIT MEDIA INDEPENDENT INTERFACE) . O segundo sub-layer, denominado PMA (Physical Medium Attachment) é responsável pela serialização e deserialização (SERDES/DESERDES) de bits de dados a partir da camada PCS no modo de transmissão e recepção. A camada PMD (Physical Medium dependent) está diretamente ligada com o módulo óptico MDI (MEDIUM DEPENDENT INTERFACE), através de um laser de transmissão ou de um foto detector na recepção.

A configuração de transmissão de dados entre as sub-camadas do padrão 1GBEthernet é ilustrada na figura 23 de forma detalhada. Percebe-se que as interfaces apresentam linhas paralelas onde as taxas são divididas, resultando em muitos problemas de sincronismo.

Configurações semelhantes para 10 Gb/s foram especificadas de acordo com o padrão IEEE 802.3, e será apresentada na próxima sessão.

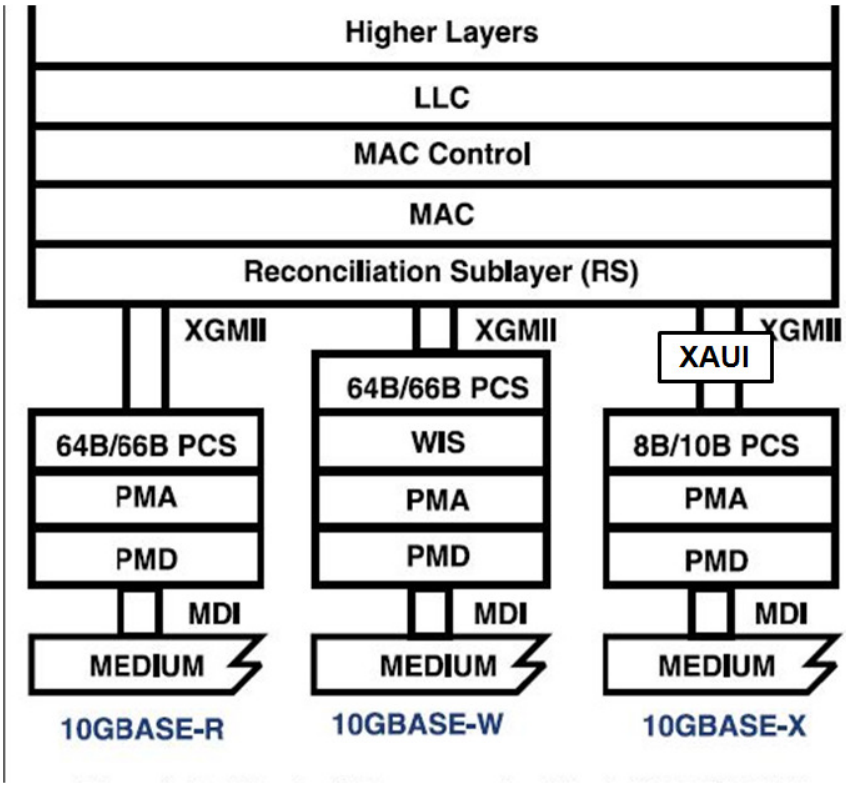


Transmissão de dados entre as sub-camadas do padrão 1GBEthernet

Ethernet 10Gb/s

No padrão 10GBE [33] uma interface denominada XGMII permite uma operação full-duplex com uma taxa de 10 Gb/s. A interface contém 74 linhas que operam em paralelo entre a camada PCS (Physical Code Sublayer) que implementa a codificação 64B/66B e a camada de reconciliação RS (Reconciliation Sublayer), nesta interface 02 blocos de 32 trilhas cada são utilizadas para informação e 10 trilhas são utilizadas para a sincronização. Penalidades devido ao efeito "Skew" (diferença do tempo de chegada de dados entre diferentes linhas paralelas) são verificadas com distâncias curtas e limitam a utilização desta interface.

Para superar esses problemas, o 10 Gigabit Ethernet Task Force desenvolveu a interface XAUI, uma interface full-duplex que utiliza quatro (4) links diferencial (sef-clocked) em cada direção para a ativação de 10 Gb/s de transferência de dados no total. Cada link serial opera em 3,125 Gb/s associados com codificação 8B/10B na camada PCS. A figura 24 apresenta as arquiteturas do padrão 10GBE PHY / LAN / WAN.

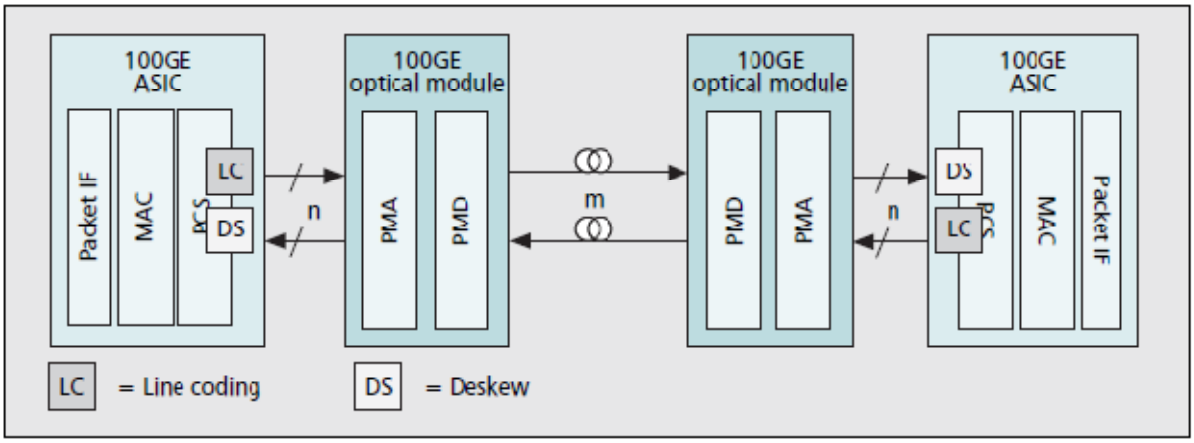


Arquiteturas do padrão 10GB Ethernet PHY / LAN / WAN

Verifica-se então que os pacotes/quadros formados nas tecnologias IP/Ethernet são processados no formato paralelo desde sua geração nas camadas superiores incluindo as conexões internas. O formato serial é utilizado somente quando estes pacotes são introduzidos no meio físico. Na taxa de 10 GBs, os problemas de "skew", sincronização de relógio e dos comprimentos envolvidos impuseram a introdução da uma camada adicional (XAUI) entre as camadas RS e PCS. Estes problemas são agravados com o aumento das taxas de bits envolvidas, como será visto a seguir.

Ethernet 100Gb/s e 40Gb/s

A figura 25 apresenta a arquitetura do padrão IEEE 802.3 ab [29,30] proposta pelo grupo HSSG - (Higher Speed Study Group) como solução da taxa de transmissão de 100Gb/s que pode ser aplicada também a taxa de 40Gb/s.



Arquitetura 100GEthernet

É muito importante observar que ASICs de alta velocidade e FPGA "Chips" implementam tarefas mais inteligentes por meio de processamento paralelo. No padrão IEEE 802.3 / 100GBE, o fluxo de dados é codificado com o código 64B/66B produzindo um sinal de 103,125 Gb / s distribuídos em 10 linhas físicas de 10,3125 Gb/s cada, multiplexadas em 20 conexões lógicas na camada PCS. A taxa de sinal de cada conexão lógica é 5,15625 Gb/s. Na sub-camada PMA, os 20 canais lógicos são convertidos em 04 linhas físicas paralelas, com 25 Gb/s de taxa individual apresentadas de acordo com a figura (26).

Os principais problemas com processamento paralelo multi-linhas são os efeitos “Skew”, sincronização de relógio e as distancias envolvidas, já verificados ma taxa de 10 GBs.

No padrão 100GBE que é especificado pelo IEEE, as camadas PCS e PMA são implementadas no mesmo “chip”. Devido a sua complexidade, a comunicação entre as camadas MAC e PCS requerem uma integração em larga escala envolvendo diversas conexões com mais de 10 milímetros de trilhas e a utilização de um numero grande de componentes de eletrônica digital. Essa implementação exige um conjunto de procedimentos

adicionais aos utilizados nas interfaces anteriormente introduzidas em 1GBE e 10GBE devido às maiores taxas de transmissão, 100Gb/s e ao complexo sistema de serialização e desserialização envolvidos.

Implementação Ethernet Board Full duplex

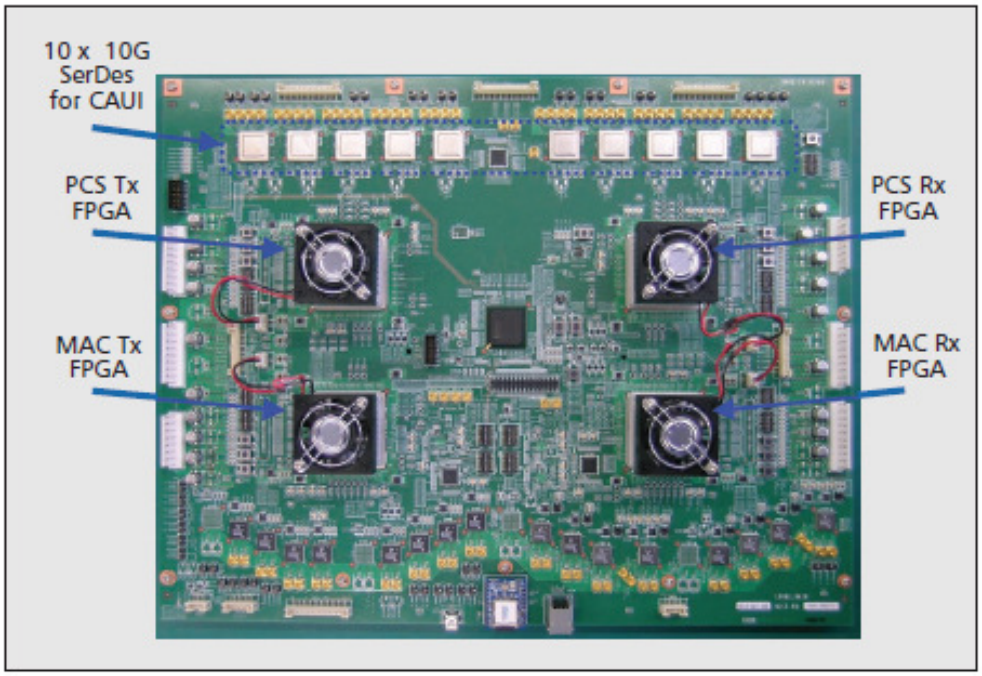
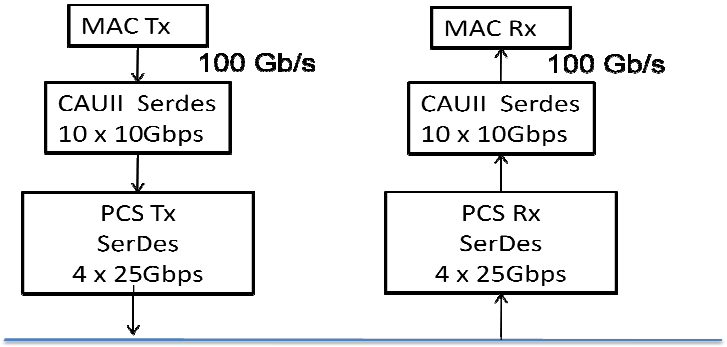


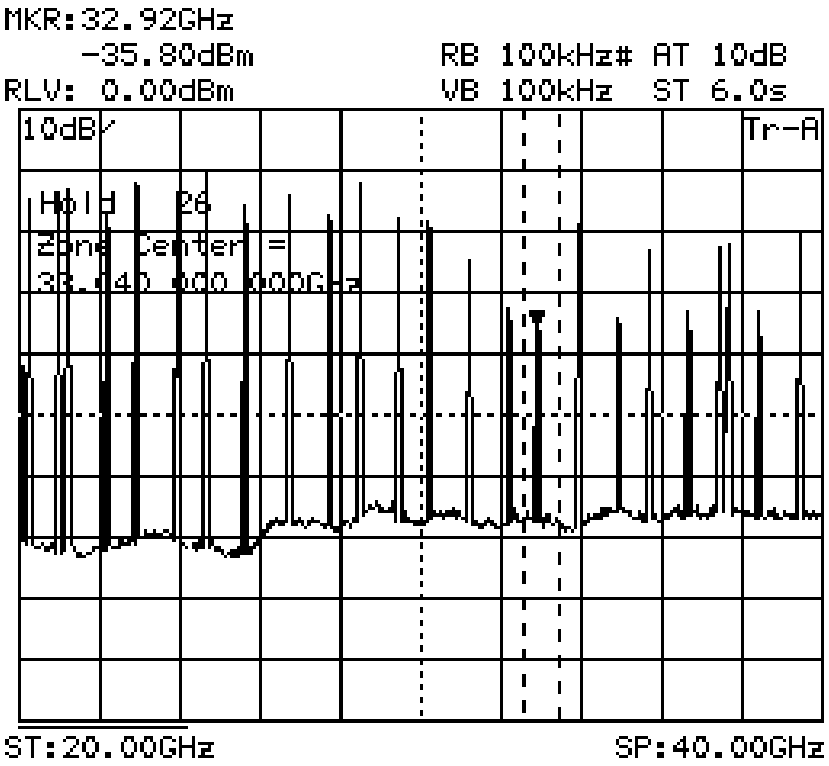
Figure 6. *Picture of the evaluation board for 100GbE MAC/PCS prototype.*

Detalhes da arquitetura 100GBE EEE P802.3ba task force

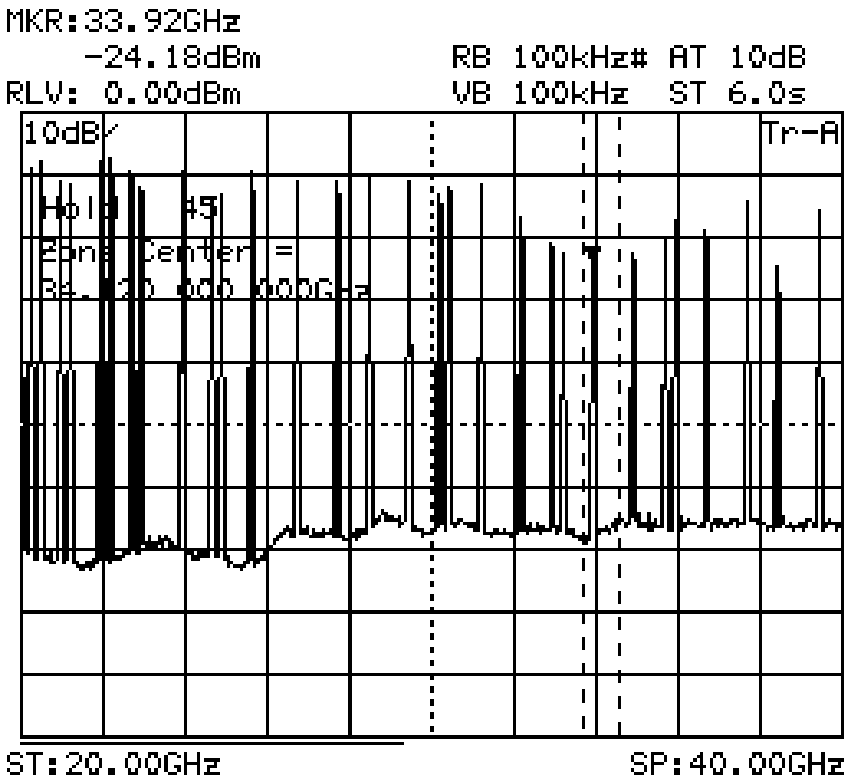


Anexo 9 - Resultado de medidas Protótipo SIWG R6010

Resultado capturado do analisador de espectro de 20-40 GHz



Protótipo 1 : vias somente com epox



Prototipo 2 : Vias com epox + fio de cobre